

## quantumdata<sup>™</sup> M42d DisplayPort 2.0 Video Analyzer/Generator



### Full 80Gb/s Link Rate Functional and Compliance Tester

#### **Key Features**

- Equipped with both DP standard and USB-C ports for Tx and Rx functions
- Test DP sources 10Gb/s,13.5Gb/s & 20Gb/s lane rates at the new 128b/132b line coding
- View incoming video and metadata—including DSC compressed--from a source device
- Capture and decode incoming video, protocol, control packets including Display Stream Compression (DSC)
- Video generator to test displays and monitors at UHBR lane rates with large format & image library
- Configure link training parameters to test display's handling of link training on video generator
- Generate Display Stream Compression (DSC), select patterns and configure slices and video parameters
- View and edit EDID and DPCD registers
- Monitor Aux Channel transactions while emulating a DP 1.4 or DP 2.0 source or sink
- Passively monitor the Main Link and Aux Channel between a source & display at all UHBR lane rates
- Run tests on source and NEW! sink devices with Panel Replay capability
- Support for LTTPR in non-transparent mode for 128b/132b at UHBR rates at 8b/10b line code for lane rates up to HBR3
- View Power Delivery (PD) protocol negotiations for USB-C DP Alt Mode
- UPDATED! DP 2.0 Link Layer compliance tests on source & sink devices up to 20.0Gb/s per lane
- NEW TESTS! DP 2.0 LTTPR compliance tests on source & sink devices up to 20.0Gb/s per lane
- UPDATED! DP Adaptive Sync compliance tests on source and sync devices
- NEW! Run DP Adaptive Sync functional tests on source and sync devices
- Run approved DP 1.4 Link Layer compliance tests on sources and sinks up to 8.1Gb/s per lane
- Run DP 1.4 Forward Error Correction (FEC) and Display Stream Compression (DSC) compliance tests for sources and sinks
- Run HDCP 2.2/3 compliance tests on DisplayPort sources, sinks and branch devices
- Run audio tests using LPCM sine wave audio tones
- Run Golden Frame PRN error tests on sources and in loopback configuration
- Run tests on embedded DisplayPort (eDP) 1.4b sources and panels (limited)
- UPDATED! Application Programming Interface (API) for automated testing for compliance & functional testing.

The Teledyne LeCroy quantumdata M42d Video Analyzer/Generator provides an unprecedented combination of functional and compliance testing for video, audio and protocol of DisplayPort 2.0 and DisplayPort 1.4. The M42d supports legacy DisplayPort lane rates of 1.62, 2.7, 5.4, 8.1 Gb/s and the new DP 2.0 higher speed lane rates and new line coding—128b/132b—of 10.0, 13.5 & 20.0Gb/s data rates up to 4 lanes. The protocol analyzer provides a snapshot status view and deep analysis using captures of incoming DisplayPort 2.0 (and DP 1.4) streams from source devices including DSC/FEC compressed streams. The M42d's video generator can be used for testing silicon development boards, displays, docking stations and hubs, USB-C adapters, extenders, etc. The video generator offers a large library of standard video timings and test patterns necessary for testing next generation high resolution displays.

The M42d supports a full suite of DP 1.4 link layer, forward error correction (FEC) and display stream compression (DSC) compliance tests for both sources and sinks. (Compliance tests for DP 2.0 are currently being implemented.)

The Passive Probe feature based on Teledyne LeCroy's cutting-edge T.A.P.4<sup>™</sup> technology, enables full monitoring of the DisplayPort Main Link and the Aux Channel between two DisplayPort devices up to 20 Gb/s lane rates future.

#### Operation

The M42d supports generation and analysis of the DisplayPort data streams through the user-friendly ATP Manager. The M42d can be controlled through the ATP Manager operated either via a laptop connected to the M42d RJ45 LAN port or through a USB keyboard and mouse and a connected UHD HDMI admin display.



## **DISPLAY TESTS - VIDEO TESTING**

#### **Video Generation**

The M42d supports video and audio functional testing at UHBR lane rates up on 1, 2 and 4 lanes to support high resolution formats. The M42d has an extensive set of video formats and library of test patterns. You can specify lane configurations for link training (below).



#### Link Training Control and Configuration



#### **Format Selection**

	Format									Refres
CTA	VESA	Folder	Lists	EDID						General
Reso	lution	Vto	otal	Frame R	ate	Aspect	4320p60			
240p2x	240p4x			24/1.001	24	Ratio	VIC 199			
288p2x	288p4x				25	4:3				
480p		314		30/1.001	30	16:9				
480p2x	480i2x			48/1.001	48	64:27				
480p4x	480i4x				50	256:135				
576p				60/1.001	60	Box				
576p2x	576i2x				100	FILL				
576p4x	576i4x			120/1.001	120	4:3				
720p										
1080p	1080i			240/1.001	240					
2160p	4320p									

#### Aux Channel Analyzer (ACA)

The M42d 's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training, MST negotiations, HDCP transactions, DP Alt Mode PD negotiations and EDID exchanges between the M42d Rx port and a connected source. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

#### Aux Channel Analyzer

	CA Data Vie	wer									
Оре	en Clo	se	Export 0	ptions	Filter Find						
21 [A	UX log wi	th 4 L	TTPR emulated	_FFE_tuning	Events: 535 (535)						
83 84 85 86 87	DNAT DNAT DNAT DNAT DNAT	13 13 13 13	+00:13:12. +00:13:12. +00:13:12. +00:13:12. +00:13:12.	664256 664330 664398 664472	< ACK 41 00 00 00 > R:90 FEC_CAPABILITY L=1 < ACK BF > R:60 DSC SUPFORT L=15 < ACK 01 21 03 7F FB 07 01 00 00 1F 0E	0		tart Time: +00:13: Type: Native Direction: Reply Command: ACK D Read Request.	12.665605		
88 89 90	DNAT DNAT DNAT	13	+00:13:12. +00:13:12. +00:13:12.	664748	<pre>&gt; R:D eDP_CONFIGURATION_CAP L=1 &lt; ACK 00 &gt; R:701 EDP_GENERAL_CAPABILITY_1 L=1</pre>	0	Bit	ATTER_FIELD_DATA_S		Value	Description
91 92 93	DNAT DNAT DNAT	13	+00:13:12. +00:13:12. +00:13:12.	664960	< ACK 87 > R:702 EDF_BACKLIGHT_ADJ_CAPS L=1 < ACK 22		7-4	Minor Revision N Major Revision N	umber	0 2	
94 95 96	DNAT DNAT DNAT	13 13	+00:13:12. +00:13:12. +00:13:12.	665101 665175	<pre>&gt; R:725 EDP_PHHGEN_BIT_COUNT_MIN L=2 &lt; ACK 02 0C &gt; R:2E FX ALPM CAPABILITIES L=1</pre>	l	Bit	3b/10b_MAX_LINK_RA Name MAX_LINK_RATE		Value	Description 8.1 Gbps/lane
97 98 99	DNAT DNAT DNAT	13 13	+00:13:12. +00:13:12. +00:13:12.	665393 665475	<pre>&lt; ACK 03 &gt; W:116 RX_ALPM_CONFIGURATION L=1 01 &lt; ACK</pre>		Bit	PHY_REPEATER_CNT Name			Description
100 101 102	DNAT DNAT DNAT	13 13	+00:13:12. +00:13:12. +00:13:12.	665605 665801	<pre>&gt; R:F0000 LTTPR_FIELD_DATA_STRUCTURE_RE &lt; ACK 20 1E 10 AA 04 10 01 05 &gt; W:F0003 PHY_REPEATER_MCDE L=1 AA</pre>	1	F0003: 1	LTTPR Count PHY_REPEATER_MODE Name		10h Value	4 Description
103 104 105	DNAT DPLT DPLT	13	+00:13:12. +00:13:12. +00:13:12.	665999	<pre>&lt; ACK &gt; W:108 MAIN_LINK_CHANNEL_CODING_SET L= &lt; ACK</pre>	1	7-0	Mode			Non-transparent
106 107 108	DPLT DPLT DPLT	13	+00:13:12. +00:13:12. +00:13:12.	666219	> W:100 LINK_BW_SET L=1 04 < ACK > W:101 LANE COUNT SET L=1 84		Bit	MAX_LANE_COUNT_PHY Name			Description
109 110 111	DPLT DPLT DPLT	13 13	+00:13:12. +00:13:12. +00:13:12.	666401 766793	< ACK > W:107 DOWNSPREAD_CTRL L=1 00 < ACK		4-0 5 6 7	MAX_LANE_COUNT		04h 0 0	
112 113 114	DNAT DNAT	13 13	+00:13:12. +00:13:12. +00:13:12.	766978 767060	<pre>&gt; W:600 SINK_SET_POWER L=1 01 &lt; ACK &gt; R:E TRAINING AUX RD INTERVAL L=1</pre>			PHY_REPEATER_EXTEN Name			Description
	and an	- 3			I - N.W ADDALLAND DOL DOL DOL	6	• <	101: < ACK 20	1E 10 AA 04 1	0 01 0	)5

#### Link Training Control and Configuration

The M41d 's link training control feature enables you to configure the link training parameters. You can set limits on the lane count and link rate and allow the link training engine to establish link training based on those limitations or you can force link training parameters—lane count, link rate, voltage swing, pre-emphasis.

## **SOURCE TESTS - VIDEO & PROTOCOL ANALYSIS**

#### **Receiver - Basic & Capture Analyzer**

The M42d 's Basic Analyzer enables you to view the incoming video, lanes and link rate, timing, colorimetry and various other metadata in real time at a glance. The Basic Analyzer mode provides a basic confidence test to verify that the incoming video is essentially correct. The Rx port emulates any EDID on to test a source devices handling of various EDIDs. You can also configure DPCD registers for emulating on the DP Rx port using the DPCD Editor.



#### Link Training Status

Tools: MyM42d	(10.30.196.34) DisplayPort/USBC 2.0 Protocol Analyzer RX - RX	$\times$
Port Status		
MST	REFRESH	
Hot-plug	RX Main Link Lane Count: 4 RX Main Link Bandwidth Setting: 10.00Gbps per lane	
HDCP	Lane 0: CR done, ChannelEQ done, Symbol locked [v0, p0]	
ALPM	Lane 1: CR done, ChannelEQ done, Symbol locked [v0, p0] Lane 2: CR done, ChannelEQ done, Symbol locked [v0, p0]	
eDP	Lane 3: CR done, ChannelEQ done, Symbol locked [v0, p0]	
USB-C		
Error Info		
Backlight		
SPDIF / Trigger		
Analysis		
	CLOSE	

#### **Receiver – Basic Analysis**



#### **Receiver - Capture Analyzer**

The deep Capture Analyzer enables you to view the protocol data of the high-speed link (shown below) and the underlying virtual channels (shown below). The Capture Analyzer provide deep insight into the data, control symbols, video, metadata and protocol data.

#### **Capture Analysis (Main Link)**

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		rames 20G_Cap										Open	Open V		iewer /	
Ope	n Segment	Rows Events	Find Time: HH:MM:SS.ms.us.ns(.	ps)	•											
0	🐮 🖑	→ ④ ④ Marker 1: □	A Marker 2:	•	>					Find	Goto	MTP		Names		
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Data										+2			0040404	20242424	20202010	
										+2	10240		0101010	1010101010	10101010	
										-1	10100		0101010	1010101010	20202020	
													0101010	1010101010	10101010	
CSB										+6	10102		0101010	1010101010	20202020	
										+7	10103		0101010	10101010	10101010	
										+8	VCE		VCPF	VCPF	VCPF	
											14140		4040404	Departante	10101010	
inors										+10	04040		1010010	04040404	10101010	
										+11	10040		0040404	10040404	10202010	
										+13	10100		0101010	10101010	10100010	
										+12	10102		0101010	10101010	10101010	
larkers										414	10102		0101010	10101010	10302010	
sancers										+15	10100	110 1	0101010	10101010	10302010	
										+16	10100		0101010	10101010	10352010	
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			Link Clock #		-					+10	10545		0040404	10040404	10101010	
e	Link Clock #	TimeStamp	Type			k Rate				+1.9	10100	140 3	0101010	10101010	10101010	
	1	0:0:0.000.000.001.650	Version Information		Lin	k Rate: 20.0Gbs	(0x22)			+20	10101	110 1	0101010	10101010	10101010	
	1	0:0:0.000.000.001.650	Link Rate Change		4					+21	10100	110 1	0101010	10101010	10101010	
	182	0:0:0.000.000.300.300	LLCP Data							+22	10103	110 1	0101010	10101010	10101010	
	193	0:0:0.000.000.318.450	Capture Trigger							+23	10100	110 3	0101010	10101010	10101010	
	65722	0:0:0.000.108.440.550	LLCP Data							+24	10103	120 2	0101010	10101010	10101010	
	131262	0:0:0.000.216.580.800	LLCP Data							+25	10103	110 1	0101010	10101010	10101010	
	196802	0:0:0.000.324.722.700	LLCP Data							+26	arara	F10 8	2626F10	889898210	82525210	
	262342	0:0:0.000.432.862.950	LLCP Data							+27	STOOD	110 5	#101010	57101010	\$ <b>F</b> 362620	
	327882	0:0:0.000.541.004.950	LLCP Data							+20	00000	000 0	0000000	00000000	66000000	
	393422	0:0:0.000.649.145.200	LLCP Data							+29	00000	000 0	0000000	00000000	00000000	
	458962	0:0:0.000.757.287.100	LLCP Data							+00		000 0	0000000	00000000	66000000	
	524502	0:0:0.000.865.427.350	LLCP Data							+21	00000	000 0	0000000	00000000	00000000	
	590042	0:0:0.000.973.569.250	LLCP Data							+22	00000	000 0	0000000	00000000	0000000	
	655582	0:0:0.001.081.709.500	LLCP Data							+33	00000	000 0	0000000	00000000	00000000	
	721122	0:0:0.001.189.849.750	LLCP Data							+04	00000	100 0	0000000	00000000	666600000	
	786662	0:0:0.001.297.991.650	LLCP Data							+25	00000	000 0	0000000	00000000	666600000	
	852202	0:0:0.001.406.132.000	LLCP Data							+26	00000	000 0	0000000	00000000	0000000	
	917742	0:0:0.001.514.273.900	LLCP Data							+27	00000	000 0	0000000	00000000	0000000	
	983282	0:0:0.001.622.414.150	LLCP Data							+23	00000	000 0	0000000	00000000	00000000	
	1048822	0:0:0.001.730.556.050	LLCP Data	10						+23	00000	000 0	0000000	00000000	66600000	
1 :	1114362	0:0:0.001.838.696.300	LLCP Data		1				2							

#### Capture Analysis – Virtual Channels

	(Data Erai	mes 11_12_2020_16_38_25 [VC	-					Open VC	Main
								openvo	Main
	Segment	Rows Events Find	Time: HH:MM:SS.ms.us.ns(.p						
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				к « < > » х	Offset	LO	L1	L2	13
			-		-16	00000000	00000000	00000000	000000000
Deta		vao	<b>600</b>		-15	00000000	00000000	00000000	000000000
					-14	00000000	00000000	00000000	000000000
					-13	00000000	00000000	00000000	000000000
CS8					-12	00000000	00000000	00000000	00000000
0.00					-11	00000000	00000000	00000000	00000000
					-10	00000000	00000000	00000000	00000000
					-9	00000000	00000000	00000000	00000000
Errors					-0	00000000	00000000	00000000	00000000
					-7	00000000	00000000	00000000	000000000
					-6	00000000	00000000	00000000	00000000
Markers					-5	00000000	00000000	00000000	0000000
					-4	00000000	00000000	00000000	000000000
31	9369	319437	319505	319573 319642	-3	00000000	00000000	00000000	00000000
			Link Clock #		-2	00000000	00000000	00000000	00000000
0863	319446	TimeStamp 0:0:0.001.971.888.889	Type SE	Picture Parameter Set Packet ID: 0		55	55	55	55
10864	319440	0:0:0.001.971.938.272	SS	# of Bytes: 7fh	+0	00120000	80200010 0000£010	001E007F	C0030000
10864								00007008	00000003
			and build a	dsc_version_major: 1	+1	02008000			
	319455	0:0:0.001.971.944.444	CTA Audio	dsc version minor: 2	+2	00580300	003FE120	COOFCOOD	00070005
10866	319458	0:0:0.001.971.944.444 0:0:0.001.971.962.963	SE	dsc version minor: 2 pps_identifier: 0	+2 +3	00580300 F0100018	003FE120 00200C03	33080806	38281018
10865 10866 10867	319458 319466	0:0:0.001.971.944.444 0:0:0.001.971.962.963 0:0:0.001.972.012.346	SE SS	dsc version minor: 2 pps_identifier: 0 bits_per_component: 8 bpc	+2 +3 +4	00580300 F0100018 62544600	003FE120 00200C03 79777000	33080806 01787D00	382A1C0E 09000100
10866 10867 10868	319458 319466 319467	0:0:0.001.971.944.444 0:0:0.001.971.962.963 0:0:0.001.972.012.346 0:0:0.001.972.018.519	SE SS VSC	dsc version minor: 2 pps_identifier: 0	+2 +3 +4 +5	00580300 P0100018 62544600 BE090069	003FE120 00200C03 79777000 EA19007B	33080806 01787D00 381A0002	382ALCO 09000100 B6220040
10866 10867 10868 10869	319458 319466 319467 319470	0:0:0.001.971.944.444 0:0:0.001.971.962.963 0:0:0.001.972.012.346 0:0:0.001.972.018.519 0:0:0.001.972.037.037	SE SS VSC SE	dsc_version_minor: 2 ppg_identifier: 0 hits_per_component: 0 bpc linebuf_depth: 16 bits block_pred_enable: Yes convert_rgb: No	+2 43 +4 +5 44	00580300 F0100018 62544600 BE090069 2A00FC19	003FE120 00200C03 79777000 FR19007B 4300F819	33080806 01787D00 381A0002 0000781A	382ALC08 09000100 B6220040 00008623
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L0866 L0867 L0868 L0869 L0870 L0871 L0872 L0872	319458 319466 319467 319470 319504 319505 319516 319973	0:0:0.001.971.944.444 0:0:0.001.971.942.963 0:0:0.001.972.012.346 0:0:0.001.972.012.346 0:0:0.001.972.013.519 0:0:0.001.972.246.914 0:0:0.001.972.320.988 0:0:0.001.972.320.988 0:0:0.001.975.141.975	SE SS VSC SS Ficture Parameter Set SE BS	dsc version minor: 2 ppm_idstriffer: 0 bits per_component: 0 bpc linebaf depth: 16 bits block pred enable: 7es block pred enable: 7es blo	+2 +3 +5 +6 +7 +8 +3 +10	00580300 F010018 62544600 BE050065 2A00FC19 007428F6 0000000 0000000 0000000	003FE120 0020C03 79777000 FA19007B 4300FE19 00746334 0000000 0000000 0000000	33080806 01787D00 381A0002 0000781A 00000000 00000000 00000000 00000000	382ALCOE 09000100 B6220040 0000862A 00000000 00000000 00000000 00000000
L0866 L0867 L0868 L0869 L0870 L0871 L0872 L0873 L0873	319458 319466 319467 319470 319504 319505 319516 319973 319974	$\begin{array}{c} 0:0:0.\ 001\ 971\ 944\ 444\\ 0:0:0.\ 001\ 971\ 962\ 963\\ 0:0:0\ 001\ 972\ 012\ 346\\ 0:0:0\ 001\ 972\ 012\ 346\\ 0:0:0\ 001\ 972\ 037\ 037\\ 0:0:0\ 001\ 972\ 037\ 037\\ 0:0:0\ 001\ 972\ 037\ 037\\ 0:0:0\ 001\ 972\ 250\ 986\\ 0:0:0\ 001\ 972\ 320\ 986\\ 0:0:0\ 001\ 975\ 144\ 975\\ 0:0:0\ 001\ 975\ 144\ 976\\ 0:0:0\ 001\ 975\ 148\ 148\\ \end{array}$	SE SS VSC SS Ficture Parameter Set SE BS BS Data	dsc_version_minor: 2 ppidentifier: 0 bits_per_component: 4 bick_per_component: 4 bick_per_dentifier conver_rpp: No simple_d2: No vfr_enable: No mattw_d2: No distribute_for tang do do tang do do tang do	+2 +3 +4 +5 +6 +7 +0 +20 +10 +11	00580300 F0100018 63544600 BE050069 2A00FC19 00042AF6 0000000 00000000 00000000 SE	003FE120 00200C03 79777000 FA19007B 4300F619 00746334 0000000 0000000 0000000 SE	33080806 01787500 38130002 00007813 0000000 0000000 0000000 0000000 SE	382A100E 09000100 B6220040 00000842A 00000000 00000000 00000000 SE
L0866 L0867 L0868 L0869 L0870 L0871 L0872 L0873 L0874 L0875	319458 319466 319467 319470 319504 319505 319516 319973 319974 320559	$\begin{array}{c} 0:0:0.001,971,944,444\\ 0:0:0.001,971,942,963\\ 0:0:0.001,972,012,946\\ 0:0:0.001,972,012,946\\ 0:0:0.001,972,013,954\\ 0:0:0.001,972,037,037\\ 0:0:0.001,972,245,914\\ 0:0:0:0.001,972,253,086\\ 0:0:0.001,975,141,975\\ 0:0:0.001,975,148,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ $	SE SS VSC SS Picture Parameter Set SE BS BS Data BS	dsc_version_minor: 2 pps_identific: 0 limber_form limber_form covert_rgb: No covert_rgb: No war and the second second second second second second second mative_400: No mative_400: No tame 3: 00 00 32 c0 80 c0 00 0 ff 00 07 06 Lane 3: 70 00 00 00 00 c0 00 00 00 07 06	+2 +3 +4 +5 +4 +7 +0 +10 +11 +12	00580300 F0100018 63544600 BE050069 2A00FC19 00042AF6 0000000 00000000 00000000 SE 00000000	003FE120 00200C03 79777000 FA19007B 4300F619 00746334 0000000 0000000 0000000 SE 0000000	3388866 01787200 8812002 00007812 0000000 0000000 0000000 0000000 SE 0000000	38281018 09000100 B6220040 00008628 00000000 00000000 00000000 SE 00000000
10866 10867 10868 10869 10870 10871 10872 10873 10874 10875 10876	319458 319466 319467 319470 319504 319505 319516 319973 319974 320559 320560	0:0:0:001.971.944.444 0:0:0:001.971.942.943 0:0:0:001.972.012.946 0:0:0:001.972.012.946 0:0:0:001.972.037.037 0:0:0:001.972.245.086 0:0:0:001.972.245.086 0:0:0:001.975.145.915 0:0:0:001.975.145.915 0:0:0:001.975.758.259	SE SS VSC SS Ficture Parameter Set SE BS BS Data BS Data	dsc_version_minor: 2 pro_identifier: 0 bits_per_component: 0 bots_per_component: 0 bots_	+2 +3 +4 +5 +4 +7 +0 +10 +11 +13	00580300 F0100318 62544600 BE050065 2A00FC19 00742AF6 0000000 00000000 00000000 SE 00000000 00000000	003FE120 00206C03 79777000 EA19007B 4300F819 00744334 0000000 00200000 00000000 SE 00000000 00000000	3080806 01787000 9812002 00007812 0000000 0000000 0000000 0000000 SE 0000000 0000000	38284008 09000100 B62200400 00008628 00000000 00000000 00000000 SE 00000000 00000000
10866 10867 10868 10870 10870 10871 10872 10873 10874 10875	319458 319466 319467 319470 319504 319505 319516 319973 319974 320559	$\begin{array}{c} 0:0:0.001,971,944,444\\ 0:0:0.001,971,942,963\\ 0:0:0.001,972,012,946\\ 0:0:0.001,972,012,946\\ 0:0:0.001,972,013,954\\ 0:0:0.001,972,037,037\\ 0:0:0.001,972,246,914\\ 0:0:0:0.001,972,246,914\\ 0:0:0:0.001,972,246,914\\ 0:0:0:0.001,972,246,914\\ 0:0:0:0.001,975,141,975\\ 0:0:0.001,975,148,975\\ 0:0:0:0.001,975,148,975\\ 0:0:0:0.001,975,148,975\\ 0:0:0:0.01,975,148,975\\ 0:0:0.001,975,148,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975\\ 0:0:0.001,975$	SE SS VSC SS Picture Parameter Set SE BS BS Data BS	dsc_version_minor: 2 pps_identific: 0 limber_form limber_form covert_rgb: No covert_rgb: No war and the second second second second second second second mative_400: No mative_400: No tame 3: 00 00 32 c0 80 c0 00 0 ff 00 07 06 Lane 3: 70 00 00 00 00 c0 00 00 00 07 06	+2 +3 +4 +5 +4 +7 +0 +10 +11 +12	00580300 F0100018 63544600 BE050069 2A00FC19 00042AF6 0000000 00000000 00000000 SE 00000000	003FE120 00200C03 79777000 FA19007B 4300F619 00746334 0000000 0000000 0000000 SE 0000000	3388866 01787200 8812002 00007812 0000000 0000000 0000000 0000000 SE 0000000	382ALCOE 09000100 B6220040 0000862A 00000000 00000000 00000000 SE 00000000

## **DP 2.0/1.4 LINK LAYER SOURCE COMPLIANCE**

#### **Source Link Layer Compliance**

The DP source link layer compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.



#### **DP 2.0 Source Link Layer Compliance Test Results**

DP 2.0 Source (Core R1.0) Compliance Test F	Rogulta			
HTML Report Instrument: MyM41h [10.30.196.36] +	N30113		CONTINUE DEST EXEC	
	Manufacturer			
Date Tested: June 7, 2021 9:44 AM	Model Name:			
Overall Status: CTS Core R1.0 - Pass	Port Tested: 1			
4.2.2.11: [Draft for DP2.0]Various UHBR AUX read interval verification in first EQ loop.		1	PASS	
<ul> <li>4.2.2.12: [Draft for DP2.0]UHBR Link Status/Adjust different FFE Request, different AUX read interval for 11</li> </ul>	0 FO loon		PASS	
<ul> <li>4.3.1.14: [Draft for DP2.0]Successful Link Training at All Supported Lane Counts and UHBR Link Speeds</li> </ul>	r Ed toop		PASS	
v aller 01:		1	PASS	
> = 01; [1] Link Training test for lane count = 1 and lane. rate = 10.00				
> G 02: [2] Link Training test for lane count = 2 and lane_rate = 10.00				
> Q 03: [3] Link Training test for lane count = 4 and lane_rate = 10.00				
> © D4: [4] Link Training test for lane count = 1 and lane_rate = 13.50				
> © 05: [5] Link Training test for lane count = 2 and lane_rate = 13.50				
o 06: [6] Link Training test for lane count = 4 and lane_rate = 13.50				
<ul> <li>Source DUT sets 128b132b encoding before TPS1 .</li> </ul>				
<ul> <li>Source DUT sets TPS0 (DPCD 102h 3:0 bits=0) to Clear Training.</li> </ul>				
<ul> <li>Source DUT sets 128b132b encoding before TPS1 .</li> </ul>				
Source DUT waits for status register 205h to verify LT termination before TPS1.				
<ul> <li>Source DUT sets expected Link Rate= 13 50Gbps.</li> </ul>				
<ul> <li>Source DUT sets expected Lane count# 0x4.</li> </ul>				
<ul> <li>Source DUT sets TPS1 (DPCD 102h 3.0 bits=1) for Training.</li> </ul>				
<ul> <li>Source DUT reads 128b132b AUX read interval register 2216h before TPS2.</li> </ul>				
<ul> <li>Source DUT Reads FFE Values Adjustment for all fanes before TPS2.</li> </ul>				
<ul> <li>Source DUT Writes FFE Values Adjustment for all lanes before TPS2.</li> </ul>				
» Source DUT sets TP2 (DPCD 102h 3:0 bits-2) for EQ Training.				
<ul> <li>Source DUL reads status register 202h to verify EO status before TPS2 CDS Sequence.</li> </ul>				
Source DUT reads status register 202h to 207h in one AUX read transaction during EQ Sequence.				
<ul> <li>Source DUT reads status register read 128b132b AUX read interval before TPS2 CDS Sequence.</li> </ul>				
<ul> <li>Source DUT waits for EO done on all lanes status before TPS2 CDS Sequence.</li> </ul>				
Open ACA Data Source DUT waits for TPS2 CDS Sequence Done before Training Finish.				_
			cu	/SE

#### DP 1.4/2.0 Source Link Layer Compliance - Test Selection

		_
DP 2.0 Source		×
strument: M	MyM41d [10.30.196.17] - Connect Cards	
	CDF Entry Test Selection Test Options / Preview	
pen Save	Select All Categories Deselect All Categories	
legory	Testa Select All Clear All	
IX Rd. er HPD	4.3.1.6: [Same as DP1.4]Successful Link Training (Higher Pre-emphasis Setting during Channel Equalization)	
ID and	4.3.1.7: [Same as DP1.4] Successful Link Training (Lower Link Rate During Channel Equalization)	
CD Rd.	4.3.1.8: [Same as DP1.4]Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing	
k Training	🗌 4.3.1.9: [Same as DP1.4]Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing 🛛 🔘	
k Maint.	4.3.1.10: [Same as DP1.4]Unsuccessful Link Training (Failure in Channel Equalization)	
eo	□ 4.3.1.11: [Same as DP1.4]Successful Link Training (Simultaneous Request for Diff. Voltage Swing/Pre-emphasis)	
ver nagement	4.3.1.12: [Same as DP1.4]Source Device Link Training CR Fallback Test	
dio	4.3.1.13: [Same as DP1.4]Source Device Link Training EQ Fallback Test	
	4.3.1.14: [Draft for DP2.0]Successful Link Training at All Supported Lane Counts and UHBR Link Speeds	
1	4.3.1.15: [Draft for DP2.0]Successful Link Training Upon HPD Plug Event for UHBR	
	4.3.1.16: [Draft for DP2.0]Successful Link Training when EQ done at 20th loop during channel EQ phase	
	4.3.1.17: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When EQ not done in 20 loop during channel EQ phase.	
	4.3.1.18: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When LT Failed received in middle of 20 loop (random 1 to 19) during channel	E
	4.3.1.19: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop during channel EQ Done.	
	4.3.1.20: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done.	
	4.3.1.21: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When EQ InterLane align done bit not set 20ms after EQ done.	
	4.3.1.22: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When Symbols not locked in (LTTPR_COUNT +1)*20ms during CDS phase.	D
	4.3.1.23: [Draft for DP2.0]Successful Link Training to a Lower Bandwidth. When CDS InterLane align done bit not set in (LTTPR_COUNT +1)*20ms during	g
	d and a second se	2

#### DP 1.4 Source Link Layer Compliance Test Results

DP 1.4 Source (1.4 Core R1.0) Compliance Test Results		
esults Name: 03_27_2018_15_33_45 Manufacturer:		HTML Rep
Date Tested: March 27, 2018 3:33 PM Model Name:		
verall Status: CTS 1.4 Core R1.0 - Pass Port Tested: 1		
Test Results		
Test Name / Details	0	Status
4.3.2.1: Successful Link Re-training After IRO HPD Pulse Due to Loss of Symbol		Pass
• Iter 01:		Pass
▶		Pass
▷		Pass
> @ 03: [3] After Sym lock error on lane 2, Link Maintenance test for lane cou		Pass
>		Pass
▲ 🥥 05: [5] After Sym lock error on lane 4, Link Maintenance test for lane cou		Pass
After loss of Symbol Lock on lane 4.		
<ul> <li>Link re-training starts after IRQ pulse.</li> </ul>		
Source DUT reads DPCD address 0200-0205h.		
Source DUT read link status within 100ms.		
Source DUT start link training		
Source DUT sets link bw and lane count before TP1 is set.		
<ul> <li>Source DUT sets TP1 on all active lanes.</li> </ul>		
<ul> <li>CR Lock succeeded on all active lanes.</li> </ul>		
Training pattern 2 or 3 or 4 detected after Training pattern 1.		
<ul> <li>For HBR3 source Training pattern 4 detected.</li> </ul>		
<ul> <li>Equalization succeeded on all active lanes.</li> </ul>		
<ul> <li>Symbol lock succeeded on all active lanes.</li> </ul>		
<ul> <li>All Lanes are Aligned and skewed.</li> </ul>		
• Link compliance training test completed successfully.		
Link training completed in 19.76 ms, which exceeds the 10ms guideline.		
4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock H		Pass
4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-		Pass
4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set.	-	Pass
1 4.3.2.5: Lane Count Reduction and Increase.	<b>-</b>	rass
Den ACA Data 4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.		
strument: [\$\$9808 [10.30.196.39]	- Þ C	ontinue Test Executio
		X Close

#### DP Aux Channel Traces – From LLC Test

Ope	n Clo	se	Export Options	Filter Find					
A	UX log w		TTPR emulated_FFE_tunin	ng] Events: 535 (535)					
333	DPLT	13	+00:13:12.885924	< ACK 77 77 05 03	0	00202 . 1	ANEO 1 STATUS:		
334	DPLT	13	+00:13:12.887189	> R:202 LANEO_1_STATUS: L=4			Name	Value	Description
335	DPLT	13	+00:13:12.887263	< ACK 77 77 05 03					
336	DPLT	13	+00:13:12.888479	> R:202 LANEO_1_STATUS: L=4		0	LANEO_CR_DONE	Y(1)	
337	DPLT	13	+00:13:12.888553	< ACK 77 77 05 03		1	LANEO CHANNEL EQ DONE LANEO SYMBOL LOCKED	Y(1) Y(1)	
338	DPLT	13	+00:13:12.889842	> R:202 LANEO_1_STATUS: L=4			LANEO_SINBOL_DOCKED	1(1)	Reserved
339	DPLT	13	+00:13:12.889916	< ACK 77 77 05 03		4	LANE1 CR DONE	Y(1)	Neserven
340	DPLT	13	+00:13:12.891175	> R:202 LANEO_1_STATUS: L=4		5	LANE1 CHANNEL EQ DONE	Y(1)	
341	DPLT	13	+00:13:12.891249	< ACK 77 77 05 03		6	LANE1_SYMBOL_LOCKED	Y(1)	
342	DPLT	13	+00:13:12.892497	> R:202 LANE0_1_STATUS: L=4		7		0	Reserved
343	DPLT	13	+00:13:12.892571	< ACK 77 77 05 03		00202- 7	ANE2 3 STATUS		
344	DPLT	13	+00:13:12.893836	> R:202 LANEO_1_STATUS: L=4			Nane	Value	Description
345	DPLT	13	+00:13:12.893910	< ACK 77 77 0D 03					
346	DPLT	13	+00:13:12.894090	> W:102 TRAINING PATTERN_SET: L=1 00		0	LANE2_CR_DONE	T(1)	
347	DPLT	13	+00:13:12.894172	< ACK		1	LANE2_CHANNEL_EQ_DONE	Y(1)	
348	DNAT	13	+00:13:12.894360	> R:200 SINK_COUNT L=6		2	LANE2_SYMBOL_LOCKED	Y(1)	Reserved
349	DNAT	13	+00:13:12.894434	< ACK 41 00 77 77 0D 02		4	LANE3 CR DONE	Y(1)	manua velu
350	DPLT	13	+00:13:12.894688	> R:100 LINK EW SET L=9		5	LANES CHANNEL EQ DONE	T(1)	
351	DPLT	13	+00:13:12.894762	< ACK 04 84 00 05 05 05 05 00 02		6	LANE3_SYMBOL_LOCKED	Y(1)	
352	DNAT	13	+00:13:12.894898	> R:200 SINK_COUNT L=8		7		0	Reserved
353	DNAT	13	+00:13:12.894972	< ACK 41 00 77 77 0D 02 66 66		00204 - 1	ANE ALIGN STATUS UPDATED		
354	DPLT	13	+00:13:12.896928	> R:100 LINK BW SET L=9	0		Name	Value	Description
355	DPLT	13	+00:13:12.897002	< ACK 04 84 00 05 05 05 05 00 02					
356	DPLT	13	+00:13:12.900671	> R:100 LINK_BW_SET L=9		0	INTERLANE_ALIGN_DONE	Y(1)	
357	DPLT	13	+00:13:12.900745	< ACK 04 84 00 05 05 05 05 00 02		1	POST_LT_ADJ_REQ_IN_PROGRESS		
358	DNAT	13	+00:13:12.974553	> R:200 SINK COUNT L=8		2	128b/132b DFRX EQ INTERLANE AL 128b/132b DFRX CDS INTERLANE A	IGN DO	NE Y(1)
359	DNAT	13	+00:13:12.974627	< ACK 41 00 77 77 0D 03 66 66		4	128b/132b LT FAILED	N(0)	una a (a)
360	DNAT	13	+00:13:13.069295	> R:200 SINK_COUNT L=8		5		0	Reserved
361	DNAT	13	+00:13:13.069369	< ACK 41 00 77 77 0D 03 66 66		6	DOWNSTREAM_PORT_STATUS_CHANGED		
362	DPLT	13	+00:13:13.149956	> R:100 LINK BW SET L=9		7	LINK_STATUS_UPDATED	N(0)	
363	DPLT	13	+00:13:13.150030	< ACK 04 84 00 05 05 05 05 00 02	_		INK STATUS		
364	DPLT	13	+00:13:13.150164	> R:100 LINK BW SET L=9	_		Name	-	Description

#### Sink Link Layer & EDID Compliance

The DP sink (display) and EDID/DisplayID and Link Layer compliance tests are ideal for pre-testing or self-testing (where permitted) your DisplayPort display product prior to submission to an Authorized Test Center for approval. Pretesting provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).



#### **DP 1.4 Link Layer Compliance - Test Selection**

일 D	P 1.4a Sink CT Core R1.0	-		$\times$
Ins	trument: AL_M41d [10.30.196.30] - Connect Cards			
	CDF Entry Test Selection Test Options	/ Preview		
Sele	ct All 🧭 🛪 Count Options	EXEC	UTE TES	STS .
×	AUX Ch. Proto.			^
>	5.2.1.1: Read One Byte from Valid DPCD Address	1	1	
>	5.2.1.2: DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	1	1	
>	5.2.1.3: Write One Byte to Valid DPCD Address	1	1	
>	5.2.1.4: Write Nine Bytes to Valid DPCD Addresses	1	1	
>	5.2.1.5: Write EDID Offset (One Byte I2C-Over-AUX Write)	1	1	
>	5.2.1.6: Read One EDID Byte (One Byte I2C-Over-AUX Read)	1	1	
>	5.2.1.7: EDID Read	1	1	
>	5.2.1.8: Illegal AUX Request Syntax	1	1	
>	5.2.1.9: Glitch Rejection	1	1	
>	5.2.1.10: Interleaved EDID and DPCD Receiver Capability Read	1	1	
>	5.2.1.11: Downstream Stop on MOT Reset	1	1	
>	5.2.1.12: Downstream Stop on Timeout	1	1	
v	Sink DPCD Field Impl.			
>	5.2.2.1: Sink Organizationally Unique Identifier (OUI)	1	1	
>	5.2.2.2: Sink Count	1	1	
>	5.2.2.3: Sink Status	1	1	
>	5.2.2.4: Sink Error Count	1	1	
>	5.2.2.5: DPCD Address Range	1	1	
>	5.2.2.6: Number of Receiver Ports	1	1	
>	5.2.2.7: Main Link Channel Coding	1	1	
>	5.2.2.8: ESI Field Mapping	1	1	

#### **DP 1.4 Link Layer Compliance - Test Results**

Compliance Test Results Viewer			
DP 1.4 Sink (	(1.4 Core R1.0) Compliance Test Results		
Results Name: 03_27_2018 15 56 17 sink	Manufacturer:		HTML Rep
Date Tested: March 27, 2018 3:56 PM	Model Name:		
Overall Status: CTS 1.4 Core R1.0 - Pass	Port Tested: 1		
	Test Results		
Test Name / Details	T Kalk Policikatika	0	Status
	All Supported Lane Counts and Link Speeds	Q	Pass
A G Iter 01:	All supported Lane Counts and Link speeds		Pass
Definition of the second se	ount = 1 and lane rate = $1.62$		Pass
02: Link Training test for lane of 02: Link Training test for lane of			Pass
> 9 03: Link Training test for lane c			Pass
04: Link Training test for lane of			Pass
05: Link Training test for lane containing			Pass
Ø 06: Link Training test for lane of			Pass
> @ 07: Link Training test for lane co			Pass
> @ 08: Link Training test for lane co			Pass
Ø 09: Link Training test for lane contains			Pass
IO: Link Training test for lane containing	ount = 1 and lane rate = 8.10		Pass
I1: Link Training test for lane containing	ount = 2 and lane rate = 8.10		Pass
I2: Link Training test for lane contains and the second	ount = 4 and lane rate = 8.10		Pass
5.3.1.2: Successful Link Training with	h Request of Higher Differential Voltage		Pass
	a Lower Link Rate Due to Clock Recovery L		Pass
	h Request of a Change to Pre-Emphasis and		Pass
4 🕞 Iter 01:			Pass
4	ount = 4 and lane rate = 8.10		Pass
<ul> <li>HPD is asserted</li> </ul>			
<ul> <li>Reference Source receives AUX_ACK at 1 a</li> </ul>			
<ul> <li>Reference Source receives AUX ACK from e</li> </ul>	either write request		
<ul> <li>AUX Read 0x2201 (MAX_LINK_RATE) = 0x1e</li> </ul>			
<ul> <li>AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4</li> <li>CR lock succeeded on lane 0</li> </ul>			
<ul> <li>CR lock succeeded on lane U</li> <li>1 iterations to achieve CR lock at VOLT/</li> </ul>	ACR FUTUR FRT - 0 on land 0		
<ul> <li>I iterations to achieve CR lock at VOLTA</li> <li>CR lock succeeded on lane 1</li> </ul>	NOD_SWING_SDI = 0 ON IANG 0		
Die Open ACA Data 5.3.1.1: Successful Link Training at All Supported L	Lane Counts and Link Speeds		
Instrument: SS980B [10.30.196.39]		• •	Continue Test Executio
			M of a
			🔀 Close



006	en Clos	e Export	Options	Filter	Find						
I IA	AV DP AC	A_Capture Eve	nte: 356 (1331								
		DF-T10	+00:30:45		NFD Falling Edge		st	art Time: +00:30:50.871183			
	DPHP	DP-T10	+00:30:50		HPD Rising Edge			Type: Native			
	DPHP	DP-T10	+00:30:50	867851	HPD Falling Edge	12	0	irection: Reply			
	DPHP	DF-T10	+00:30:50	867852	HPD Rising Edge			Command: ACK			
	DNAT	DF-T10	+00:30:50	868068	> R:200 SINK COUNT L=6		Reply to	Read Request.			
	DNAT	DP-T10	+00:30:50	868141	< ACK 41 04 00 00 80 00			P1.3 DPCD REV			
	DNAT	DF-T10	+00:30:50	870824	> R:E TRAINING AUX RD INTERVAL L=1			Name	Walter	Description	
	DNAT	DP-T10	+00:30:50	870897	< ACK 81					Description	į
	DNAT	DF-TIO	+00:30:50	870966	> B:0 DPCD REV L=1			Minor Revision	4		
	DNAT	DF-T10	+00:30:50	871039	< ACK 14		7-4	Major Revision	1		
0	DNAT	DF-710	+00:30:50	871110	> 8:2200 DP1.3 DPCD REV L=16			AX LINK RATE			
1	DNAT	DP-T10	+00:30:50	871183	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08			Name	Value	Description	
2	DNAT	DF-710	+00:30:50	871393	> R:90 FEC CAPABILITY L=1						ļ
3	DNAT	DP-710	+00:30:50	871466	< ACK BF		7-0	MAX_LINK_RATE	1Eh	8.1 Gbps/lan	ł
4	DNAT	DP-TIO	+00:30:50	871544	> R:60 DSC SUPPORT L#15			and the second			
5	DNAT	DF-T10	+00:30:50	871617	< ACK 01 21 03 7F FB 07 01 00 00 1F 0E EE			NAME_COUNT	-	Description	
6	DNAT	DF-T10	+00:30:50	871906	> R:D eDF CONFIGURATION CAF L=1		MAG	/14.75#	AWTON	Description	
7	DNAT	DP-T10	+00:30:50	871979	< ACK 00			MAX LANE COUNT	4	4 lanes	
8	DNAT	DF-T10	+00:30:50	872047	> R:701 EDF GENERAL CAPABILITY 1 L=1		5	POST_LT_ADJ_REQ_SUP	N(0)		
9	DNAT	DP-T10	+00:30:50	872120	< ACK 87			TPS3_SUPPORTED	¥(1)		
0	DNAT	DF-T10	+00:30:50	872188	> R:702 EDF BACKLIGHT ADJ CAPS L=1		7	ENHANCED_FRAME_CAP	T(1)		
1	DNAT	DF-T10	+00:30:50	872261	< ACK 22		02203: M	AX DOWNSPREAD			
2	DNAT	DP-710	+00:30:50	872331	> R:725 EDP FWMGEN BIT COUNT MIN L=2			Name	Value	Description	
3	DNAT	DF-T10	+00:30:50	872403	< ACK 02 0C						
	DNAT	DP-T10	+00:30:50	872482	> R:2E RX ALPM CAPABILITIES L=1		0	MAK_DOWNSPREAD STREAM REGEN STATUS CAP		Up to 0.5%	
5	DNAT	DP-T10	+00:30:50	872554	< ACK 03		1	STREAM_REGEN_STATUS_CAP	N(0)	Reserved	
6	DNAT	DP-T10	+00:30:50	872624	> W:116 RX ALPH CONFIGURATION L=1 01		3		0	Reserved	
7	DNAT	DF-T10	+00:30:50	872704	< ACK		4		0	Reserved	
в	DHDCP	DF-710	+00:30:50	873436	> R:69493 RxStatus L=1		5		0	Reserved	
9	DEDCP	DF-T10	+00:30:50	873509	< ACK 00			NO_AUX_HANDSHAKE_LINK_TRAININ			
0	DFL/T	DF-T10	+00:30:50	935325	> R:100 LINK_BM_SET L=2		7	TPS4_SUPPORTED	T(1)		
1	DPLT	DP-TI0	+00:30:50	935398	< ACK 1E 04		02204: N	ORP			
2	DNAT	DF-T10	+00:30:51	030734	> R:200 SINK_COUNT L=6			Name	Value	Description	
3	DNAT	DP-T10	+00:30:51	030807	< ACK 41 04 00 00 00 00		<				

## **ADAPTIVE SYNC FUNCTIONAL TESTING**

#### Adaptive Sync Source Functional Testing

The M42d now supports the testing of Adaptive Sync-capable source and sink devices for HBR3 rates. The Adaptive Sync analyzer for testing Adaptive Sync-capable source devices enables you to view the variations in the vertical blanking to lower the refresh rate. The Adaptive Sync video generation for testing Adaptive Sync-capable displays or monitors enables you to send different test patterns that increase and decrease the vertical blanking to increase or decrease the refresh rate of the display. Adaptive Sync testing for sink devices is currently only supported through the command line with GUI support to be provided in the future.

#### **Adaptive Sync Capture Analysis**

You can view the Adaptive Sync variations in the vertical blanking in the Capture Analyzer as shown below.

#### Adapative Sync Aux Channel Analyzer (ACA)

You can view the Adaptive Sync discover and configuration transactions occurring over the Aux Channel with the Aux Channel Analyzer (ACA) as shown left.

256 1 257 1 258 1 259 1 260 1 261 1 262 1 263 1 263 1 264 1	DI2C DI2C DI2C DI2C DPLT DPLT DPLT DPLT	DP-R12 DP-R12 DP-R12 DP-R12 DP-R12 DP-R12 DP-R12	+01:02:11.5615 +01:02:11.5619 +01:02:11.5625 +01:02:11.5625 +01:02:11.5862 +01:02:11.5863	967 524 598 229	> R:AD EDID L=16 < DEFER > R:AD EDID L=16 < ACK 00 00 00 00 00 00 00 00 00 00 00 00 00	•	Start Time: +01:02:16.021352 Type: Native			
257 1 258 1 259 1 260 1 261 1 262 1 263 1 263 1 264 1 265 1	DI2C DI2C DI2C DPLT DPLT DPLT DPLT	DP-R12 DP-R12 DP-R12 DP-R12 DP-R12 DP-R12 DP-R12	+01:02:11.5619 +01:02:11.5625 +01:02:11.5625 +01:02:11.5862 +01:02:11.5863	967 524 598 229	< DEFER > R:A0 EDID L=16	۰	Type: Native			
258 1 259 1 260 1 261 1 262 1 263 1 263 1 264 1 265 1	DI2C DI2C DPLT DPLT DPLT DPLT	DP-R12 DP-R12 DP-R12 DP-R12 DP-R12	+01:02:11.5625 +01:02:11.5625 +01:02:11.5862 +01:02:11.5863	524 598 229	> R:AO EDID L=16					
259 1 260 1 261 1 262 1 263 1 264 1 265 1	DI2C DPLT DPLT DPLT DPLT	DP-R12 DP-R12 DP-R12 DP-R12	+01:02:11.5625 +01:02:11.5862 +01:02:11.5863	598 229						
260 1 261 1 262 1 263 1 264 1 265 1	DPLT DPLT DPLT DPLT	DP-R12 DP-R12 DP-R12	+01:02:11.5862 +01:02:11.5863	229	< ACK 00 00 00 00 00 00 00 00 00 00 00 00 00		Direction: Request Command: Write			
261 1 262 1 263 1 264 1 265 1	DPLT DPLT DPLT	DP-R12 DP-R12	+01:02:11.5863				Address: 0x00107 (DOWNSPREAD )	CTRL		
262 1 263 1 264 1 265 1	DPLT	DP-R12			> R:100 LINK BW SET L=9		Length: 1	,,		
263 1 264 1 265 1	DPLT			303	< ACK 1E 84 00 08 08 08 08 00 01	۲				
264 I 265 I			+01:02:12.0803	390	> R:100 LINK BW SET L=9		00107: DOWNSPREAD CTRL			
265 1	DNAT	DP-R12	+01:02:12.0804	164	< ACK 1E 84 00 08 08 08 08 00 01		Bit Name	Value	Descrip	tion
		DP-R12	+01:02:12.1894	171	> R:2214 FEATURE ENUMERATION LIST CONT L=1		0	0	Reserve	
	DNAT	DP-R12	+01:02:12.1895	545	< ACK 03		1		Reserve	
266 1	DNAT	DP-R12	+01:02:12.1896	512	> R:7 DOWN STREAM FORT COUNT L=1		2		Reserve	
267 1	DNAT	DP-R12	+01:02:12.1896	586	< ACK 44		3		Reserve	đ
268 1	DPLT	DP-R12	+01:02:12.1897	155	> R:107 DOWNSPREAD CTRL L=1		4 SPREAD_AMP	N(O)		
269 1	DPLT	DP-R12	+01:02:12.1898		< ACK 00		5 6 ADAPTIVE SYNC SDP EN	0 N(D)	Reserve	
270 1	DPLT	DP-R12	+01:02:16.0213	352	> W:107 DOWNSPREAD CTRL L=1 80			Y(1)		
271 1	DPLT	DP-R12	+01:02:16.0214		< ACK		[0000][80 01 07 00 80][	1		
272 1	DPLT	DP-R12	+01:02:17.3788	324	> R:107 DOWNSPREAD CTRL L=1					
273 1	DPLT	DP-R12	+01:02:17.3788	198	< ACK 80					
274 1	DPLT	DP-R12	+01:02:33.0243	307	> R:100 LINK BW SET L=9					
275 1	DPLT	DP-R12	+01:02:33.0243	381	< ACK 1E 84 00 08 08 08 08 80 01					
276 1	DPLT	DP-R12	+01:02:33.2161	137	> R:100 LINK BW SET L=9					
277 1	DPLT	DP-R12	+01:02:33.2162	211	< ACK 1E 84 00 08 08 08 08 80 01					
278 1	DPHP	DP-R12	+01:03:24.1640	182	HPD Falling Edge					
279 1	DPHP	DP-R12	+01:03:25.1641	101	HPD Rising Edge					
280 1	DNAT	DP-R12	+01:03:25.1643	390	> R:200 SINK COUNT L=6					
281 1	DNAT	DP-R12	+01:03:25.1644	164	< ACK 41 00 22 22 81 00					
282 1	DNAT	DP-R12	+01:03:25.1645	579	> R:E TRAINING AUX RD INTERVAL L=1					
283 1	DNAT	DP-R12	+01:03:25.1646	53	< ACK 81					
284 1	DNAT	DP-R12	+01:03:25.1647	17	> R:0 DPCD_REV L-1					
285 1	DNAT	DP-R12	+01:03:25.1647	791	< ACK 14					
286 1	DNAT	DP-R12	+01:03:25.1648	159	> R:2200 DP1.3_DPCD_REV L=16					
287 1	DNAT	DP-R12	+01:03:25.1649	33	< ACK 14 1E C4 80 01 00 01 40 00 20 04 08 00 00 81 00					
288 1	DNAT	DP-R12	+01:03:25.1651	40	> R:2210 DPRX_FEATURE_ENUMERATION_LIST L=16					
289 1	DNAT	DP-R12	+01:03:25.1652	214	< ACK 0A 00 00 00 03 00 85 00 00 00 00 00 00 00 00 00					
290 1	DNAT	DP-R12	+01:03:25.1654	123	> R:90 FEC_CAPABILITY L=1					
291 1	DNAT	DP-R12	+01:03:25.1654	97	< ACK BE					
292 1	DNAT	DP-R12	+01:03:25.1655	566	> R:60 DSC SUPPORT L=16					
293 1	DNAT	DP-R12	+01:03:25.1656	540	< ACK 00 21 03 7F FB 07 01 00 00 1F 0E EE 08 07 00 00					
294 1	DNAT	DP-R12	+01:03:25.1658	165	> R:D eDP_CONFIGURATION_CAP L=1					
295 1	DNAT	DP-R12	+01:03:25.1659	39	< ACK 00					
296 1	DNAT	DP-R12	+01:03:25.1660	14	> R:701 EDP_GENERAL_CAPABILITY_1 L=1					
297 1	DNAT	DP-R12	+01:03:25.1660	188	< ACK 87					



## **ADAPTIVE SYNC COMPLIANCE TESTS**

#### Adaptive Sync Source Compliance Test Selection

C DP Adaptive-Sync Source CT R1.0		x c
Instrument: MyM41h [10.30.196.186] 🗢 Connect Cards		
CDF Entry Test Selection Test Options / Prev	iew	
Select All 🧭 🕷 Count Options	EXECUTE	TESTS
<ul> <li>Fixed Average VTotal</li> </ul>		
> 4.8.1.1: Fixed Average VTotal Support over the Declared Frame Rate Range	1	1
> 4.8.1.2: Duration Increase Constraint Value Support	1	1
<ul> <li>Adaptive VTotal</li> </ul>		
> 4.8.2.1: Adaptive VTotal Support with Duration Increase Constraint Value	1	1
> 4.8.2.2: Adaptive VTotal Support with Unconstrained Duration Increase	1	1
	CL	OSE

#### Adaptive Sync Sink Compliance Test Selection

DP Adaptive-Sync Sink CT R1.0 -	- 🗆	×
Instrument: MyM41h [10.30.196.186] 🗢 Connect Cards		
CDF Entry Test Selection Test Options / Previ	ew	
Select All 🧭 💥 Count Options	XECUTE	TESTS
<ul> <li>Adaptive-Sync Operation</li> </ul>		
5.8.1.1: Fixed Average VTotal Support over the Declared Frame Rate Range	1	1
<ul> <li>5.8.1.2: Duration Increase Constraint Value Support</li> </ul>	1	1
> 5.8.1.3: Adaptive VTotal Support	1	1
	CLO	DSE

#### Adaptive Sync Compliance Testing

The M42d supports Adaptive Sync compliance testing for both source and sink devices. The examples below (source left, sink right) show the details provided with the compliance test results. Currently tests are provided for rates up to HBR3 with UHBR support coming in a future release.

#### Adaptive Sync Source Compliance Test Results

E Compliance Test Results Viewer			- 0	×	
	rnc Source (R1.0) Compliance Test Results				
HTML Report Instrument: MyM41h [10.30.196.186] 🗢			CONTINUE TEST EXECUT	ION	
Results Name: M42d_AS_LL_Source	Manufacturer:				
Date Tested: January 13, 2022 3:59 PM	Model Name:				
Overall Status: CTS R1.0 - Pass	Port Tested: 1				
4.8.1.1: Fixed Average VTotal Support over the Decla	red Frame Rate Range	1	PASS		
4.8.1.2: Duration Increase Constraint Value Support		1	PASS		
4.8.2.1: Adaptive VTotal Support with Duration Increase		1	PASS		
<ul> <li>4.8.2.2: Adaptive VTotal Support with Unconstrained</li> </ul>	Duration Increase	1	PASS		
✓ O Iter 01:	-	1	PASS		
> 01: Verify Source DUT reads entire EDID.	within a Advention Operation		PASS		
<ul> <li>02: Verify Source DUT reads DPCD capability registers des</li> <li>02: Verify Source DUT reads 14: MOA THANKO DAD (ONO)</li> </ul>			PASS		Adaptive Sync
O3: Verify Source DUT writes 1 to MSA_TIMING_PAR_IGNO	-		PASS		Sink Test
✓ ○ 04: Verify Source DUT sends video stream with all the timin DUT link trained at Lana Count: 4 Link Data: 8 10 Chap.	ig parameters except viotal matching the		PASS		
<ul> <li>DUT link trained at: Lane Count: 4 Link Rate: 8.10 Gbps</li> <li>Testing timing: 1920x1080 (2000x1157) @ 144Hz RB3.</li> </ul>					Results
<ul> <li>Measured timing: 1920x 1030 (2000x 137) (@ 144m2 Rbs.</li> <li>Measured timing: 800 Compliance Test Results Viewer</li> </ul>					- 🗆 X
Source DUT did not or	DD Marking Come Cick (D1	0) (1	t D14-		
	DP Adaptive-Sync Sink (R1 MyM41h [10.30.196.186] マ	.u) compliance les	t Results		CONTINUE TEST EXECUTION
Lines in all a shart the string	, , , ,				
OSer Indicated that Im Results Name: M42d_AS_LL_Sink_De O5: Verify Source DUT se Date Tested: January 7, 2022 2:40 F		Manufacturer: Model Name:			
Solution of the second sec	M	Port Tested: 1			
	e VTotal Support over the Declared Fram			1	PASS
5.0.1.1. FIXEU AVERAY	ease Constraint Value Support	le Rate Ralige		1	PASS
<ul> <li>OQ: Vorify VTotal during</li> </ul>				1	PASS
<ul> <li>5.8.1.3: Adaptive VTo</li> <li>Giter 01:</li> </ul>	tai Support			1	
	ains Adaptive-Sync Operation Mode and Range d	locariptor for each C		· ·	PASS
	ync test pattern is displayed without corruption.				PASS
					PASS
	1920 x 1080 @ 144 Progressive (RGB 4:4:4).	Colculations (0v90)	36)		
	eld equals to the Reference Source's internal CRC	`	·		
	eld equals to the Reference Source's internal CRC				
	ield equals to the Reference Source's internal CR		'		
	t image looks fine for format 1920 x 1080 @ 144	+ Progressive (RGB 4	.4.4).		
	te is changing as expected.				PASS
<ul> <li>User indicated that</li> </ul>	t the Refresh Rate is changing as expected.				
Open ACA Data 5.8.1.1: Fixed Ave	rage VTotal Support over the Declared Frame Rate Range				
					CLOSE

## **DP 2.0 LTTPR SOURCE COMPLIANCE**

#### LTTPR-Capable Source Compliance

The DP Source Link Training Tunable Phy Repeater (LTTPR) compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.



#### **DP 2.0 Source LTTPR Compliance - Test Selection**

trument: My	M41h [10.30.196.186	<ul> <li>Connect Cards</li> </ul>							
	COF Er	try		Test Selection		Test Options / Prev	cw.		
		Deselect All Categories							
	Teots						Select All	Clear Al	1
r HPD				Supported Lane Counts and Link Speeds	·				
and	4.9.1.2: [Draft	in DP2.0[With 2 emulated LTTP	R, Successful Link Training at all !	Supported Lane Counts and Link Speeds	0				
D Rd.	🗌 4.9.1.3: [Draft	in DP2.0)With 3 emulated LTTP	R, Successful Link Training at all !	Supported Lane Counts and Link Speeds	٥				
Training	🗌 4.9.1.4: (Draft	in DP2.0]With 4 emulated LTTP	R, Successful Link Training at all !	Supported Lane Counts and Link Speeds	0				
Maint.	4.9.1.5: [Draft	in DP2.0]With 5 emulated LTTP	R. Successful Link Training at all !	Supported Lane Counts and Link Speeds	0				
20	() 4.9.1.6: [Draft	in DP2.0]With 6 emulated LTTP	R, Successful Link Training at all !	Supported Lane Counts and Link Speeds	0				
er agement	🗌 4.9.1.7: [Draft	in DP2.0]With 7 emulated LTTP	R, Successful Link Training at all !	Supported Lane Counts and Link Speeds	0				
•	() 4.9.1.8: [Draft	in DP2.0]With 8 emulated LTTP	R, Successful Link Training at all !	Supported Lane Counts and Link Speeds	0				
	🗌 4.9.1.9: [Draft	in DP2.0]With random[1-8] num	ber of emulated LTTPR, Successf	ul Link Training at all Supported Lane Co	unts and Link Speeds, Sink suppo	rt 4 lane and all rates.			
	🗌 4.9.1.10: [Draf	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training at all Supported Lane C	ounts and Link Speeds, LTTPR su	pport 4 lane and all rates. (	5		
PR	( 4.9.1.11: [Drat	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training (Higher Differential Vol	age Swing during Clock Recovery	0			
	() 4.9.1.12: [Drat	t in DP2.0[With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training to a Lower Link Rate/B	V#1: Iterate at Maximum Voltage	Swing 🛈			
	() 4.9.1.13: [Drai	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training to a Lower Link Rate/B	V #2: Iterate at Minimum Voltage	Swing ()			
	🗌 4.9.1.14: [Drai	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training (Higher Pre-emphasis S	etting during Channel Equalization	n) ()			
	- 4.9.1.15: [Draf	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training (Lower Link Rate/BW D	uring Channel Equalization)				
	() 4.9.1.16: [Drai	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training when EQ done at 20th l	oop during channel EQ phase	D			
	🗌 4.9.1.17: [Dra	t in DP2.0[With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training to a Lower Bandwidth, v	then CHANNEL_EQ_DONE bits no	ot set in 20 loops during chan	nel EQ phase.	0	
	() 4.9.1.18: [Drai	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training to a Lower Bandwidth. )	When LT Failed received in middle	of 20 loop (random value 1 t	19) during chan	nel EQ Done	•
	🗌 4.9.1.19: [Drai	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training to a Lower Bandwidth.	When LT Failed received at 20th lo	op during channel EQ Done.	0		
	a 4.9.1.20: [Draf	t in DP2.0]With random[1-8] nur	nber of emulated LTTPR, Success	ful Link Training to a Lower Bandwidth.	When LT Failed received at after E	Q done.			

#### DP 2.0 Source LTTPR Compliance Test Results

Number Name         Market           4.9.1.16:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.17:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.18:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.18:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.21:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.22:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.23:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.23:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.23:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.24:         [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.25:         [Draft in DP2.0]With random[1-8] number of e	Compliance Test Results Viewer		- 🗆 X
Heads Name: LTTPR_ser_4.51.16, 43.122 Data Insteir March 2022 27 AM Manufactane: March 2022 27 AM March 2022 27 AM	DP 2.0 Source (Core R1.0) Compliance Test Results		
Table Table 130 Parts         Marking           4.9.1.16: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.16: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.16: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.18: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.24: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training         1         PASS           4.9.1.25: [Draft in DP2.0]With random[1-8] number of emulat	HTML Report Instrument: MyM41h [10.30.196.186] 👻		CONTINUE TEST EXECUTION
Owned Handle State     Dest Family       4.9.1.16:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.17:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.17:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.13:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.21:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.22:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.22:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       4.9.1.22:     [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1     PASS       • 0.01:     [Link Training tet for lane court - 4 and lane_rate = 10.0     -     1     PASS       • 02:     [2] Link Training tet for lane court - 4 and lane_rate = 20.00     PASS     -     1     PASS       • 03:     [3] Link Training tet for lane court - 4 and lane_rate = 20.00     -     -     1     PASS       • 04:     [3] Link Training tet for lane court - 4 and lane_rate = 12.50     - <t< td=""><td>Results Name: LTTPR_src_4.9.1.16_4.9.1.23 Manufacturer:</td><td></td><td></td></t<>	Results Name: LTTPR_src_4.9.1.16_4.9.1.23 Manufacturer:		
4.9.1.16: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.17: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.18: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.19: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.19: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.24: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.25: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 PASS     4.9.1.25: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training     1 FTPR mode - Non-Tangement     4. Winther of LTTPRs - 6     5.00rce DUT stats register 205 bits withy LT termination before TP52.     5.00rce DUT stats register 205 bits withy LT termination before			
4.9.1.17: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.18: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.18: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.20: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         • 0.01: [Link Training test for lane court - 4 and nan_rate = 10.00       -       PASS         • 00: [Link Training test for lane court - 4 and nan_rate = 13.90       -       PASS         • 00: [Ultr Raining test for lane court - 4 and nan_rate = 12.00       PASS       -       PASS         • 00: [Ultr Raining test for lane court - 4 and nan_rate = 12.00       PASS       <			
4 9.1.18:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4 9.1.19:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4 9.1.20:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4 9.1.20:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4 9.1.22:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4 9.1.22:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4 9.1.23:       [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         • 01:       [DItth Training test for lane court - 4 and lane_state = 10.00       -       1       PASS         • 00:       [DItth TTPR]       [Ditth Training test for lane court - 4 and lane_state = 20.00       PASS       PASS         • 00:       [DItth Training test for lane court - 4 and lane_state = 20.00       PASS       PASS       PASS         • 00:       [DItth Training test for lane court - 4 and lane_state = 20.00       PASS       PASS       PASS       PASS       PASS       PASS <td< td=""><td></td><td>1</td><td>PASS ^</td></td<>		1	PASS ^
4.9.1.19: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.20: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         • 0.11 [Link Training test for lane court - 4 and nan_rate = 10.00       -       1       PASS         • 0.02 [2] Link Training test for lane court - 4 and nan_rate = 13.50       PASS       PASS         • 0.02 [2] Link Training test for lane court - 4 and nan_rate = 14.50       PASS       PASS         • 0.02 [2] Link Training test for lane court - 4 and nan_rate = 12.50       PASS       PASS         • 0.02 [2] Link Training test for lane court - 4 and nan_rate = 12.50       PASS       PASS         • 0.02 [2] Link Training test for lane court - 4 and nan_rate = 12.50       PASS       PASS		1	PASS
4.9.1.20: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training       1       PASS         • 0 Int 01:       Them count - 4 and nan_rate - 1000       -       1       PASS         • 0 02: [D1: Training test for lane count - 4 and nan_rate - 13.00       PASS       PASS         • 00: 20: B1: Training test for lane count - 4 and nan_rate - 20.00       PASS       PASS         • 00: 20: B1: Test Training test for lane count - 4 and nan_rate - 20.00       PASS       PASS         • 00: 20: B1: Test Training test for lane count - 4.4 and nan_rate - 20.00       PASS       PASS         • 00: B1: D1: test TPS0 (PCD 102h 30 bits-0] to Clear Training       Image: Clear Annormality - 20.00       PASS         • Source DUT rates expected Link Rate- apparent       Successful Link Training test for lane count- 0.4.       Sucres DUT sets appeted Link Clear Mark and thereal training       Image: Clear Mark and training         • Source DUT rates appatent Line Advisor Training       Sucres DUT sets appeted Link and thereal tofter TPS2.       Source DUT rates appatent Line before TPS2.       <	> 4.9.1.18: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training	1	PASS
49.1.21: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1	> 4.9.1.19: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training	1	PASS
49.1.22: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     1     PASS     4.9.1.23: [Draft in DP2.0]With random[1:8] number of emulated LTTPR, Successful Link Training     5.9.0.22: [Dift in Training test for lane court - 4 and lane_pate = 20.00     9.0.20: DIf wasts opecide Link Rate = 20.000ps.     5.9.0.20: DIf wasts opecide Link Rate and Link Rate Rate Rate Rate Rate Rate Rate Rate	> 4.9.1.20: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training	1	PASS
<ul> <li>             49.1.32: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful LInk Training             1             PASS             1             1</li></ul>	> 4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training	1	PASS
• Other 01:       1       PASS         • ○ 01: 01: Uture Training test for lane count + 4 and lane_rate = 10.00       PASS         • ○ 02: 21: Uture Training test for lane count + 4 and lane_rate = 13.50       PASS         • ○ 03: 30: Uture Training test for lane count + 4 and lane_rate = 13.50       PASS         • ○ 03: 30: Uture Training test for lane count + 4 and lane_rate = 20.00       PASS         • ○ 03: 30: Uture Training test for lane count + 4 and lane_rate = 20.00       PASS         • ■ Source DUT sets PR00 (PCC0 1021 30 bits / 00 Clear Training       PASS         • ■ UTTPR mode + Non-Trainsparent       ■         • ■ Winter OUT sets expected Lane count - 4 and lane_rate = 100.00       PASS         • ■ Source DUT sets expected Line Count - 604       ■         • ■ Source DUT sets expected Line Count - 004       ■         • ■ Source DUT sets expected Line Count - 1000       ■         • ■ Source DUT sets expected Line Count - 1000       ■         • ■ Source DUT sets expected Line Count - 004       ■         • ■ Source DUT sets T26: (PCD 1023 30 bits-2) for CB Training       ■         • ■ Source DUT sets T26: (PCD 1021 30 bits-2) for CD Taning       ■         • ■ Source DUT sets T26: (PCD 1021 30 bits-2) for CD Sequence.       ■         • ■ Source DUT sets T20: (PCD 1021 30 bits-2) for CD Sequence.       ■         • ■ Source DUT sets tabut setstat	> 4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training	1	PASS
> ○ 01:11 Line Training test for lane court - 4 and lane_rate = 10.00     PASS       > ○ 02:21 Line Training test for lane court - 4 and lane_rate = 13.50     PASS       > ○ 03:21 Line Training test for lane court - 4 and lane_rate = 20.00     PASS       > ○ 03:21 Line Training test for lane court - 4 and lane_rate = 20.00     PASS       > ○ 03:21 Line Training test for lane court - 4 and lane_rate = 20.00     PASS       > ○ 03:21 Line Training test for lane court - 4 and lane_rate = 20.00     PASS       > ○ UTP Statistic PS0 (PCD 102h 30 bits-0) to Chert Training     PASS       > □ UTP Fractione - Non-Trainagarentt     PASS       > ○ Source DUT sets reported Line Rate - 20.006ps.     Source DUT sets reported Line Rate - 20.006ps.       > ○ Source DUT sets reported Line Rate - 20.006ps.     Source DUT sets reported Line court- 0.4       > ○ Source DUT sets TPS1 (PCD 102h 30 bits-1) for Training.     Source DUT sets TPS1 (PCD 102h 30 bits-1) for Training.       > ○ Source DUT sets TPS1 (PCD 102h 30 bits-1) for Caning.     Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.       > ○ Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.     Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.       > ○ Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.     Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.       > ○ Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.     Source DUT sets TPS1 (PCD 102h 30 bits-2) for CD Training.       > ○ Source DUT reads status register 202h to 207h in one AUX read		1	PASS
> ○ 02: 2[ Line: Training test for lane court - 4 and lane_pate = 13.50     PASS       > ○ 03: 5[ Line: Training test for lane court - 4 and lane_pate = 13.50     PASS       > ○ 03: 5[ Line: Training test for lane court - 4 and lane_pate = 13.50     PASS       > ○ 04: 5[ Line: Training test for lane court - 4 and lane_pate = 13.50     PASS       > ○ 05: 5[ Line: Training test for lane court - 4 and lane_pate = 13.50     PASS       > ○ 05: 5[ Line: Training test for lane court - 4 and lane_pate = 13.50     PASS       > ○ 05: 5[ Line: Training test for lane court - 4 and lane; test = 75.00     PASS       > ○ 05: 50 UUT waits tespecide Line: Courts - 05.4     Source DUT sets expected Line: Courts - 05.4       > ○ 05: 50 UUT waits 128: 1326 AUX read interval register 2216 bidror TPS2.     Source DUT sets TP2 (DPCD 102:h 30 bits-4) for F1 Training       > ○ 05: 50 UUT waits T28: 1326 AUX read interval register 2216 bidror TPS2.     Source DUT reads status register 2216 bidror TPS2.       > ○ 05: 50 UUT waits T28: 126 Dit 20: 70 rE D Training.     Source DUT reads status register 2216 bidror TPS2.       > ○ 05: 50 UUT waits T28: 126 Dit 20: 70 rE D Training.     Source DUT reads status register 2216 bidror TPS2.       > ○ 05: 50 UUT waits 50 register 2216 bidror TPS2.     Source DUT reads status register 2216 bidror TPS2.       > ○ 05: 50 UUT waits 50 relinser 20: 50 to 1027h in one AUX read transaction during EQ Sequence.     Source DUT reads status register 2216 bidror TPS2.       > ○ 05: 50 UUT waits 50 relinsere 2216 Dit 20: 50 relinsere 226 Disequence.     Sou		- 1	PASS
Col: Bit Link: Training test for tane court - 4 and tane_pate = 20.00     Source DUT sets TPS0 (DPC0 120:h 30 bits=0) to Clear Training.     UTPR mode - Non-Transparent     Mumber of UTPRes = 6     Source DUT waits or status register 205h to verify L' termination before TPS1.     Source DUT sets expected Link Rate - 20.000pc.     Source DUT sets expected CINC Rate - 20.0000pc.     Source DUT sets expected			PASS
Source DUT ests TPS0 (DPC0 102h 30 bits-0) to Clear Training.     UTFR mode + Non-Yransparent     Source DUT watter for status register 2006 to verify L1 termination before TPS1.     Source DUT watter sequence link Rate + 2000 clogs.     Source DUT ests expected link Rate + 2000 clogs.     Source DUT sets expected link Rate + 200 clogs.     Source DUT sets expected link Clogs expected.     Sourc			PASS
ITTPR mode = Non-Transparent     Number of TITPRs = 6     Source DUT waits for status register 205h to verify LT termination before TPS1.     Source DUT sets expected in an count- 0-0.     Source DUT sets expected in an one- 0-0.     Source DUT sets expected in an one- 0-0.     Source DUT sets expected in an single AUX transaction.     Source DUT made 1782 (DPC 102h 30 bits-7) for ED Training.     Source DUT made status register 2010 bits-7) for ED Training.     Source DUT made status register 2010 bits-7) for ED Training.     Source DUT made status register 2010 bits-7) for ED Training.     Source DUT made status register 2010 bits-7) for ED Training.     Source DUT made status register 2010 bits-7) for CD Status before TPS2 CDS Sequence.     Source DUT made status register 2010 bits 2010 bits-7) for CDS sequence.     Source DUT waits for ED done on all innes status before TPS2 CDS Sequence.     Source DUT waits for SecUPE TPS2 CDS Sequence.     Source DUT made status register 2020 bits 204. Xu read interval before TPS2 CDS Sequence.     Source DUT made status register 2020 bits 204. Xu read interval before TPS2 CDS Sequence.     Source DUT made TS100 Differ TPS2 CDS Sequence.     Source DUT fields the CD done to differ CDS sequence of Training.     Source DUT fields the CD 200 Differ S52 OVER Sequence.     Source DUT fields the CD 200 Differ S52 OVER Sequence of Training.     Source DUT fields the CD 200 Differ S52 OVER Sequence of Training.     Source DUT fields the CD 200 Differ S52 OVER Sequence of Training.     Open ACA Data     41120 [Dan			PASS
Surve of UT THYS = 6     Source DUT waits for status register 205h to verify LT termination before TPS1.     Source DUT sets expected Link Rate - 20 0006ps.     Source DUT sets expected Link Rate - 20 0006ps.     Source DUT sets register 2010 the set expected Link Rate - 20 0006ps.     Source DUT sets register 2010 the set expected Link Rate - 20 0006ps.     Source DUT sets TPS1 (DPC 1012h 30 bits-1) for Taining.     Source DUT reads TS12 bit32 bi	<ul> <li>Source DUT sets TPS0 (DPCD 102h 3:0 bits=0) to Clear Training.</li> </ul>		
Source DUT waits for status register 205h to verify LT termination before TP61.     Source DUT and sequenced Link Rate - 20 0005pt.     Source DUT sets expected Link Rate - 20 0005pt.     Source DUT sets expected Link Rate - 20 0005pt.     Source DUT sets TP51 (DPCD 102h 30 bits-1) for Taining.     Source DUT mains 1781:0000 Tradit Sequence Register 2216 before TP62.     Source DUT mains 1781:0000 Tradit Sequence Register 2216 before TP62.     Source DUT mains 1781:0000 Tradit Sequence Register 2216 before TP62.     Source DUT mains 1781:0000 Tradit Sequence Register 2216 before TP62.     Source DUT mains 1781:0000 Tradit Sequence Register 2216 before TP62. CDS Sequence.     Source DUT mains tradit Sequence Register 2020 to 207h or RATE Register 207h or RATE Register 207h to 207h or RATE Register 207h or RATE Register 207h or RAT	<ul> <li>LTTPR mode = Non-Transparent</li> </ul>		
Source DUT sets expected Link Rate 20 000pc.     Source DUT sets expected Link Rate 20 000pc.     Source DUT sets TPSI (DPCD 102h 30 bits-1) for Training.     Source DUT sets TPSI (DPCD 102h 30 bits-2) for 21 hoters TPS2.     Source DUT sets TPSI (DPCD 102h 30 bits-2) for 22 hoters TPS2.     Source DUT sets TPSI (DPCD 102h 30 bits-2) for 20 hoters TPS2.     Source DUT sets TPSI (DPCD 102h 30 bits-2) for 20 hoters TPS2.     Source DUT sets Strained Satura register 20 hoters TPS2.     Source DUT sets Strained Satura register 20 hoters TPS2.     Source DUT sets Strained Satura register 20 hoters TPS2.     Source DUT reads status register 20 hoters TPS2.     Source DUT reads status register 20 hoters TPS2.     Source DUT reads status register 20 hoters TPS2. CDS Sequence.     Source DUT wates TPS2 (DPS 102h 30 bits-3) for CDS Sequence.     Source DUT wates DUT wates TPS2. CDS Sequence.     Source DUT wates TPS2 (DPS 102h 30 bits-3) for CDS Sequence.     Source DUT wates TPS2 (DPS 102h 30 bits-3) for CDS Sequence.     Source DUT wates TPS2 (DPS 102h 30 bits-3) for CDS Sequence.     Source DUT sets TPS1 (DPCD 102h 30 bits-3) for CDS Sequence.     Source DUT fields Channel EQ under 450 ms (actual time £290 bits).     Source DUT fields Channel EQ under 450 ms (actual time £290 bits).     Source DUT sets TPS1 (DPCD 102h 30 bits-3) for CDS Sequence.     Source DUT fields Channel EQ under 450 ms (actual time £290 bits).     Source DUT sets TPS1 (DPCD 102h 30 bits-3) for CDS Sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD 12h 30 bits-3) for CDS sequence.     Source DUT sets TPS1 (DPCD	<ul> <li>Number of LTTPRs = 6</li> </ul>		
Source DUT sets expected Lane count- 0x4     Source DUT sets expected Lane count- 0x4     Source DUT sets 1791 (DPC0 1023 3 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for Training.     Source DUT sets 1791 (DPC0 1023 bits-1) for the AUX read mataction during ED Sequence.     Source DUT reads status register 2023 to 2071 for advite the Training ED Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT waits for Instaina EQ done bit teffore TPS2 CDS Sequence.     Source DUT waits for Instaina EQ done bit teffore TPS2 CDS Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0 1023 bits-1) FOR 2005 Sequence.     Source DUT sets 1791 (DPC0			
Source DUT sets TPSI (DPCD 102:3 b Dists-1) for Training.     Source DUT reads TPSI (DPCD 102:3 b Dists-1) for Training.     Source DUT reads TPSI (DPCD 102:3 b Dists-2) for ED Training.     Source DUT reads TPS (DPCD 102:3 b Dists-2) for ED Training.     Source DUT reads TPS (DPCD 102:3 b Dists-2) for ED Training.     Source DUT reads TPSI (DPCD 102:3 b Dists-2) for ED Training.     Source DUT reads status register 20:01 to verify ED attacts before TPS2.     Source DUT reads status register 20:01 to verify ED attacts before TPS2. CDS Sequence.     Source DUT reads status register read 12:05 13:22 AUX read interval before TPS2 CDS Sequence.     Source DUT watab reads une status before TPS2 CDS Sequence.     Source DUT watab reads to DFS2.     Source DUT watab register Read 12:05 13:22 AUX read interval before TPS2 CDS Sequence.     Source DUT watab register Read 12:05 13:22 AUX read interval before TPS2 CDS Sequence.     Source DUT watab register Read 12:05 13:22 AUX read interval before TPS2 CDS Sequence.     Source DUT watab register Read 12:05 13:22 AUX read interval before TPS2 CDS Sequence.     Source DUT watab register Read 12:05 13:22 AUX read interval before TPS2 CDS Sequence.     Source DUT watab register Read 12:05 13:20 AUX read interval before TPS2 CDS Sequence.     Source DUT watab register Read 12:05 13:00 Lines 13:00 CPS AUX read interval before TPS2 CDS Sequence.     Source DUT finisher CDanne DEQ under 450 ms (actual time £390us).     Source DUT finisher CD1:02 his Dists-30; for CDS Sequence of Training.     Open ACA Data     41:120 [Dark his DFS2]; for CDS Sequence of maining 14; for the resol of the top 14; for the res			
Source DUT mains 12801320 AUX read interval register 2216h before TPS2.     Source DUT Reads FFE Values Adjustment of register 2216h before TPS2.     Source DUT Reads FFE Values Adjustment of register 2018 inter before TPS2.     Source DUT wates that register 22018 or with CPS attacts before TPS2. CDS Sequence.     Source DUT reads status register 22018 to with CPS attacts before TPS2. CDS Sequence.     Source DUT reads status register 22018 to with CPS2.     Source DUT reads status register 22018 to with CPS2.     Source DUT reads status register 22018 to with CPS2.     Source DUT reads status register 22018 to with CPS2.     Source DUT reads status register 22018 to With CPS2.     Source DUT reads status register 22018 to With CPS2.     Source DUT reads status register 22018 to With CPS2.     Source DUT reads status register 22018 to With CPS2.     Source DUT wates for temperative CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT metals CD1.     Source DUT wates for temperate CS down the Verter TPS2.     Source DUT metals TPS3.     Source DUT metals CD1.     Source DUT sets TPS3.     Source D			
Source DUT Reads FFE Values Adjustment for all lanes before TP52.     Source DUT reads TFE Values Adjustment for all lanes before TP52.     Source DUT reads status register 2021 to 2016 in a single ALX transaction.     Source DUT reads status register 2021 to 2016 in a single ALX transaction.     Source DUT reads status register 2021 to 2016 in one AUX read transaction during EQ Sequence.     Source DUT reads status register 2021 to 2016 in one AUX read transaction during EQ Sequence.     Source DUT waits DFC Dotoen on all lanes status before TP52 CDS Sequence.     Source DUT waits for EQ done on all lanes status before TP52 CDS Sequence.     Source DUT waits for lanes to EQ done to fore TP52 CDS Sequence.     Source DUT waits for lanes to EQ done to fore TP52 CDS Sequence.     Source DUT waits for lanes (CG done to fore TP52 CDS Sequence.     Source DUT waits for lanes (CG done to CG Sequence OT Frazion).     Source DUT waits for lanes (CG done to CG Sequence OT Frazion).     Source DUT waits for lanes (CG done to CG sequence OT fraining .     Qenn ACA Data     41 to [20th th EP2](birth nation[14] number of enviolated tTTP5, baccestal Link Training to a Lower Bandwidth. When UT Faled received at after EQ done.			
Source DUT sets 1792 (DPCD 102h 30 bite=2) for ED Training.     Source DUT writes DPCD 00102h through 00106h in a single AUX trainsaction.     Source DUT reads status register 202h to 207h in one AUX trainsaction druing ED Sequence.     Source DUT reads status register 202h to 207h in one AUX read transaction druing ED Sequence.     Source DUT reads status register 202h AUX read trainsaction druing ED Sequence.     Source DUT reads status register 202h AUX read trainsaction druing ED Sequence.     Source DUT reads status register 202h AUX read trainsaction druing ED Sequence.     Source DUT watch for ED done on all innes status before TPS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner PFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner PFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner PFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner PFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner RFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner RFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner RFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner RFS2 CDS Sequence.     Source DUT watch for telestere EQ done the dreiner RFS2 CDS Sequence.     Source DUT main telestere et al.     Source DUT faints dreiner EQ done the dreiner RFS2 CDS Sequence.     Source DUT faints dreiner EQ done the dreiner RFS2 CDS Sequence.     Source DUT faints dreiner EQ done the dreiner RFS2 CDS Sequence of Training.     Optim ACA DIM     Source DUT faints dreiner environment of the dreiner envi	<ul> <li>Source DUT reads 128b132b AUX read interval register 2216h before TPS2.</li> </ul>		
Source DUT writes DPCD 00102h through 00106h in a single AUX transaction.     Source DUT wates status register 2201 to 201 hore AUX rest stransaction during EQ Sequence.     Source DUT wates status register 201 to 201 hore AUX rest stransaction during EQ Sequence.     Source DUT wates status register zero 1200 hore AUX rest stransaction during EQ Sequence.     Source DUT wates status register zero 1200 hore AUX rest stransaction during EQ Sequence.     Source DUT wates for Initiation EQ conduct tedfore TPS2 CDS Sequence.     Source DUT wates for Initiation EQ done bit tedfore TPS2 CDS Sequence.     Source DUT wates for Initiation EQ done bit tedfore TPS2 CDS Sequence.     Source DUT wates for Initiation EQ done bit tedfore TPS2 CDS Sequence.     Source DUT wates for Initiation EQ done bit tedfore TPS2 CDS Sequence.     Source DUT wates for Initiation EQ done bit tedfore TPS2 CDS Sequence.     Source DUT wates for Initiation EQ done bit tedfore TPS2 CDS Sequence.     Source DUT state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source DUT state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source DUT state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source DUT state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source DUT state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source D14 state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source D14 state TS2 (CDC D120 hore) State TS2 (CDS Sequence CDT Taining).     Source D14 state TS2 (CDC D120 hore) State TS2 (CDC Sequence) State TS3 (CDC Seque			
Source DUT reads status register 202h to 207h for an AUX read transaction during EQ Sequence.     Source DUT reads status register 202h to 207h in one AUX read transaction during EQ Sequence.     Source DUT watis status register Add 128h 1320 AUX read interval before TPS2 CDS Sequence.     Source DUT watis for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT watis for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT watis for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT watis for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT watis for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT watis for intervales EQ done bit before TPS2 CDS Sequence.     Source DUT watis for intervales EQ done bit before TPS2 CDS Sequence.     Source DUT watis for intervales EQ done bit before TPS2 CDS Sequence.     Source DUT watis for intervales EQ done bit before TPS2 CDS Sequence.     Source DUT watis for intervales EQ done bit before CPS2 CDS Sequence.     Source DUT watis for intervales EQ done bit before TPS2 CDS Sequence.     Source DUT finished Channel EQ under 450 ms (actual time £290µs).     Source DUT finished Channel EQ under 450 ms (actual time £290µs).     Source DUT state TS2 (CDS Sequence of Training .     Open ACA Data     413 20 [Daft in DP22]With modingf1]mode of maining to Lower Bandwidth. When UT failed received at after EQ done.			
Source DUT reads status register 202h to 207h in one AUX read transaction during EQ Sequence.     Source DUT reads status register read 128h 132b AUX read interval leffore TPS2 CDS Sequence.     Source DUT waits for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT waits for EQ one on all lanes status before TPS2 CDS Sequence.     Source DUT maits for EQ one of all lanes status before TPS2 CDS Sequence.     Source DUT maits for EQ OUT 54 57b (20 CCC Sequence et all before TPS2 CDS Sequence.     Source DUT maits for EQ OUT 54 57b (20 CCC Sequence et all before TPS2 CDS Sequence et all before TPS2 CDS Sequence et all before TPS2 CDS Sequence.     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £290ub).     Source DUT finished Channel EQ onder 450 ms (actual time £200ub).     Source DUT finished Channel EQ onder 450 ms (actual time £200ub).     Source DUT finished Channel EQ onder 450 ms (actual time £200ub).     Source DUT finished Channel EQ onder 450 ms (actual time £200ub).     Source DUT finished Channel EQ onder 450 ms (actual time £200ub).     Source DUT finished Channel EQ onder 450	· ·		
Source DUT reads status register read 128b132b AUX read interval before TPS2 CDS Sequence.     Source DUT waits for EQ done on all lanes status before TPS2 CDS Sequence.     Source DUT waits for interlance EQ done bit before TPS2 CDS Sequence PL and the Sequence.     Source DUT waits for interlance EQ done bit before TPS2 CDS Sequence PL and the Sequence.     Source DUT waits for interlance EQ done bit before TPS2 CDS Sequence PL and the Sequence.     Source DUT waits for interlance EQ done bit before TPS2 CDS Sequence PL and the Sequence.     Source DUT waits for interlance EQ done bit before TPS2 CDS Sequence PL and the Sequence.     Source DUT sets TPS2 (PCO DUT 30 as 501=35) (PCO Sequence OT Training .     Open ACA Data     49.120 [bright in DP20]With random[16] number of emulated tTTPR, Successful Link Training to a Lower Bandwidth. When tT Failed received at after EQ done.			
Source DUT waits for EQ done on all lanes status before TPS2 CDS Sequence.     Source DUT waits for intertance EQ done bit before TPS2 CDS Sequence.     Source DUT finished Channel EQ under 450 ms (actual time 6299us).     Source DUT sets TP3 (DPCD 102h 30 bits=30 (or CDS sequence of Training .      Cpcm ACA Data     49.120 [Seit in 0P2/0Wth redom]+8] number of emulated 11TPR, biocessful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done.			
Source DUT waits for interfane EQ done bit before TPS2 CDS Sequence.     Source DUT finished Channel EQ under 450 ms (actual time (299us)).     Source DUT finished Channel EQ under 450 ms (actual time (299us)).     Source DUT sets TP3 (2000 T123 20 bits?) (CCO Sequence content of thining .     Com ACA Data     49.120 [bit in EP2/Bitti nation[1-8] number of emulated UTTPR, Successful Link Training to a Lower Bandwidth. When UT Failed received at after EQ dow.			
Source DUT finished Channel EQ under 450 ms (actual time 6299us).     Source DUT sets TP3 (DPCD 102h 30 bits~3) for CDS sequence of Training .      Cpcm ACA Data     48.120; [brift in DP2/(With random)]-8] number of emulated UTPR, Buccessful Link Training to a Lower Bandwidth, When UT Failed received at after EQ done.	<ul> <li>Source DUT waits for EQ done on all lanes status before TPS2 CDS Sequence.</li> </ul>		
Source DUT sets TP3 (DPCD 102h 30 bits-3) for CDS sequence of Training .  Cpcm ACA Data     49.120; [bart in DP2/(With random)]-8] number of emulated UTPP, Buccessful Link Training to a Lower Bandwidth. When UT Failed received at after EQ dow.	<ul> <li>Source DUT waits for interlane EQ done bit before TPS2 CDS Sequence.</li> </ul>		
Open ACA Data 49.120: [Draft in DP2.0] with random [1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done.			
	<ul> <li>Source DUT sets TP3 (DPCD 102h 3:0 bits=3) for CDS sequence of Training.</li> </ul>		
	Open ACA Data 4.9.1.20: [Draft in DP2.0] With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth. When LT Fai	led received at after EQ done.	
			CLOSE

#### DP Aux Channel Traces – From LTTPR Test

EII AC	A Data View	er					173	
Op	en Clo	se Export	Options	Filter Find				
GIL	ACA-4.9.1	16.01 Events: 131	B (3860)					
0	DPHP	DFUSBC-R13	+00:38:08.7048	13 HFD Falling Edge	Start Time: +00:38:09.976104			
1	DPHP	DPUSBC-R13	+00:38:09.8058	10 HPD Rising Edge	Type: Native			
2	DNAT	DPUSBC-R13	+00:38:09.812	11 > R:200 SINK COUNT L=6	Command: ACK			
3	DNAT	DPUSBC-R13	+00:38:09.8128	55 ACK 41 00 00 00 80 00	Reply to Read Request.			
4	DNAT	DPUSBC-R13	+00:38:09.8130	LO > R:E TRAINING AUX RD INTERVAL L=1	Rebly to Read Rednest.			
5	DNAT	DPUSBC-R13	+00:38:09.8130	34 < ACK 81	F0000: LTTPR FIELD DATA STRUCTURE REV			
6	DNAT	DPUSBC-R13	+00:38:09.813	58 > R:0 DPCD REV L=1	Bit Name	Value	Descript	ion
7	DNAT	DPUSBC-R13	+00:38:09.8132	12 < ACK 14	*****			
8	DNAT	DPUSBC-R13	+00:38:09.8133	19 > R:2200 DP1.3 DPCD REV L-16	3-0 Minor Revision Number	2		
9	DNAT	DPUSBC-R13	+00:38:09.813	ACK 14 1E C4 81 01 00 03 40 00 20 04 08 00	7-4 Major Revision Number			
10	DNAT	DPUSBC-R13	+00:38:09.813	S6 > R:2210 DPRX FEATURE ENUMERATION LIST L-16	F0001: 8b/10b MAX LINK RATE PHY REPEATED	R		
11	DNAT	DPUSBC-R13	+00:38:09.813	4 ACK 0A 00 00 00 01 01 85 00 00 00 00 00 00	Bit Name	Value	Descript	ion
12	DNAT	DPUSBC-R13	+00:38:09.813	54 > R:90 FEC CAPABILITY L=1	7-0 MAX LINK RATE		8.1 Gbps	
13	DNAT	DPUSBC-R13	+00:38:09.8140	EO < ACK BE	7-0 MAA_LINK_RATE	160	0.1 (k0)8	/1.82
14	DNAT	DPUSBC-R13	+00:38:09.8141	12 > R:60 DSC SUPPORT L=16	F0002: PHY REPEATER CNT			
15	DNAT	DPUSBC-R13	+00:38:09.814	46 < ACK 00 21 03 7F FB 07 01 00 00 1F DE EE 08	Bit Name	Value	Descript	ion
16	DNAT	DPUSBC-R13	+00:38:09.814	28 > R:D eDP CONFIGURATION CAP L=1	7-0 LTTPR Count	ROD		
17	DNAT	DPUSBC-R13	+00:38:09.814	22 < ACK 00	7-0 LTIPH COUNT	oun	*	
18	DNAT	DPUSBC-R13	+00:38:09.8145	39 > R:701 EDP_GENERAL_CAPABILITY_1 L=1	F0003: PHY REPEATER MODE			
19	DNAT	DPUSBC-R13	+00:38:09.814	53 < ACK 87	Bit Name		Descript	ion
20	DNAT	DPUSBC-R13	+00:38:09.814	10 > R:702 EDP BACKLIGHT ADJ CAPS L=1	7-0. Mode		Transpar	
21	DNAT	DPUSBC-R13	+00:38:09.8148	4 < ACK 22	/~u Mode	550	transpar	ent
22	DNAT	DPUSBC-R13	+00:38:09.814	3 > R:725 EDF FWMGEN BIT COUNT MIN L=2	F0004: MAX LANE COUNT PHY REPEATER			
23	DNAT	DPUSBC-R13	+00:38:09.814	77 < ACK 02 0C	Bit Name	Value	Descript	ion
24	DNAT	DPUSBC-R13	+00:38:09.8150	76 R:2E RX_ALPM_CAPABILITIES L=1	4-0 MAX LANE COUNT	0.45	Four lan	
25	DNAT	DPUSBC-R13	+00:38:09.815	50 < ACK 03	5		Reserved	
26	DNAT	DPUSBC-R13	+00:38:09.815	38 > W:116 RX_ALPM_CONFIGURATION L=1 01	6		Reserved	
27	DNAT	DPUSBC-R13	+00:38:09.815	20 < ACK	7	0	Reserved	
28	DNAT	DPUSBC-R13	+00:38:09.815	11 R:2214 FEATURE_ENUMERATION_LIST_CONT L=1	FOODS: PHY REPEATER EXTENDED WARE TIMEO	07		
29	DNAT	DPUSBC-R13	+00:38:09.8154	75 < ACK 01	Bit Name		Descript	ion
30	DNAT	DPUSBC-R13	+00:38:09.815	57 > R:7 DOWN_STREAM_PORT_COUNT L=1				
31	DNAT	DPUSBC-R13	+00:38:09.815		6-0 EXT_WARE_TIMEOUT_REQUEST	16		
32	DNAT	DPUSBC-R13	+00:38:09.815	29 R:7 DOWN_STREAM_PORT_COUNT L=1	7 EXT_WARE_TIMEOUT_GRANT	N(0)		
33	DNAT	DPUSBC-R13	+00:38:09.8158	33 < ACK 40	FOODS: MAIN LINK CHANNEL CODING PHY REPI	BATER		
34	DNAT		+00:38:09.9760		Bit Name		Descript	ion
35	DNAT	DPUSBC-R13	+00:38:09.976					
36	DNAT	DPUSBC-R13	+00:38:09.976	W: FOODS PHY REPEATER MODE L=1 55	0 128b/132b SUPPORTED	Y(1)		
					35: < ACK 20 1E 80 55 04	1 10 01	01	

## **DP 2.0 LTTPR SINK/DEVICE COMPLIANCE**

#### LTTPR-Capable Sink & LTTPR Device Compliance

The DP Sink and Device Link Training Tunable Phy Repeater (LTTPR) compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.

#### **DP 2.0 LTTPR Device Compliance - Test Selection**

	DP 2.0 Sink (C	Core R1.0) Compliance Test Results	
HTML Report	Instrument: MyM41h [10.30.196.186] 🗢		CONTINUE TEST EXECUTIO
Results Name: 2LTT	PR_5.9.1.13_to_5.9.1.15	Manufacturer	
	sh 14, 2022 3:35 PM	Model Name:	
Overall Status: CTS		Port Tested: 1	
	nk Training test for lane count = 4 and lane, rate = 20.00		PASS
	D is asserted		
	PR reports correct structure revision (DPCD F0000h = 0)		
	PR capability supports the link rate and lane count current	ently under test	
	erence Source receives AUX_ACK at 1 attempts		
	erence Source receives AUX ACK from either write reque		
<ul> <li>Sini</li> </ul>	k DUT Capability supports UHBR RATE = 20.00 Gbps an	id MAX_LANE_COUNT = 4	
	erence Source sets TPS0 (DPCD 102h 3.0 bits=0) to Clea		
o INT	RAHOP_AUX_REPLY_INDICATION bit clears before the 1	80ms timer expired.	
<ul> <li>Ref</li> </ul>	erence Source sets 128b132b encoding before TPS1.		
	erence Source sets Link Rate = 20.00Gbps.		
<ul> <li>Ref</li> </ul>	erence Source sets Lane count= 0x4.		
<ul> <li>Ref</li> </ul>	erence Source sets LTTPR Non-Transparent Mode (0xA/	A).	
<ul> <li>Ref</li> </ul>	erence Source sets TPS1 (DPCD 102h 3:0 bits=1) for Tra	ining.	
<ul> <li>Sinl</li> </ul>	k DUT reports 128b132b AUX read interval=6 secs (DPC	D 2216h) before TPS2.	
<ul> <li>Sinl</li> </ul>	k DUT reports FFE Values[lane0:0, lane1:0, lane2:0, lane3	3.0] Adjustments for all lanes before	
• 128	3b132b_DP_LT_FAILED bit (DPCD 204h bit 4) is NOT set I	before EQ loop	
• 128	3b132b_DP_DPRX_EQ_INTERLANE_ALIGN_DONE bit (DP	CD 204h bit 2) is NOT set before EQ	
• 128	3b132b_DP_DPRX_CDS_INTERLANE_ALIGN_DONE bit (D	PCD 204h bit 3) is NOT set before EC	
• INT	RAHOP_AUX_REPLY_INDICATION bit is clear		
<ul> <li>Ref</li> </ul>	erence Source sets TP2 (DPCD 102h 3:0 bits=2) for EQ T	raining .	
<ul> <li>Sini</li> </ul>	k DUT reports EQ done Status, Symbol lock Status [(lane	e0:1,0), (lane1:1,0), (lane2:1,0), (lane3:	
<ul> <li>Inte</li> </ul>	rlane CDS is not locked, as expected, before TPS0.		
• Ref	erence Source reads the same lane status 250 times be	fore setting TPS0.	
<ul> <li>Sint</li> </ul>	k DUT sets the LT_Failed bit (DPCD 204h bit 4=1) and th	e Reference Source sets TPS0 (DPCE	
o INT	RAHOP_AUX_REPLY_INDICATION bit clears before the 1	80ms timer expired.	
<ul> <li>Ref</li> </ul>	erence Source sets 128b132b encoding before TPS1.		
. Ref	erence Source reduces the bandwidth after link training	failed (Lane Count = 4, Link Rate = 1:	
• Ref	erence Source sets TPS1 (DPCD 102h 3:0 bits=1) for Tra	ining.	
<ul> <li>Sinl</li> </ul>	k DUT reports 128b132b AUX read interval=6 secs (DPC	D 2216h) before TPS2.	
- 1	5.9.1.13: [Draft in DP2.0]LTTPR 128b132b non-transparent successf		interes in

#### **DP 2.0 LTTPR Device Compliance - Test Results**

DD 9 0 LEPEDD Date	ice (Core R1.0) Compliance Test Results		
HTML Report Instrument: MyM41h [10.30.196.186] -	the (core stro) comprision rest message		CONTINUE TEST EXECUTIO
esults Name: LTTPR_Device_HBR_UHBR	Manufacturer:		
Date Tested: February 16, 2022 4:58 AM	Model Name:		
verall Status: CTS Core R1.0 - Pass	Port Tested: 1		
7.1.3.8: [Draft in DP2.0]With 7 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
7.1.4.1: [Draft in DP2.0]With 0 emulated LTTPR, Successfu	I Link Training at all Supported Li	1	PASS
7.1.4.2: [Draft in DP2.0]With 1 emulated LTTPR, Successful	Link Training at all Supported L	1	PASS
7.1.4.3: [Draft in DP2.0]With 2 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
7.1.4.4: [Draft in DP2.0]With 3 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
7.1.4.5: [Draft in DP2.0]With 4 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
7.1.4.6: [Draft in DP2.0]With 5 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
7.1.4.7: [Draft in DP2.0]With 6 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
7.1.4.8: [Draft in DP2.0]With 7 emulated LTTPR, Successful	I Link Training at all Supported Li	1	PASS
🗸 😳 Iter 01:	-	1	PASS
> O1: [1] Link Training test for lane count = 1 and lane_rate = 10.00			PASS
3 O2: [2] Link Training test for lane count = 2 and lane_rate = 10.00			
> O3: [3] Link Training test for lane count = 4 and lane_rate = 10.00			
> O4: [4] Link Training test for lane count = 1 and lane_rate = 13.50			
> O5: [5] Link Training test for lane count = 2 and lane_rate = 13.50			
> O6: [6] Link Training test for lane count = 4 and lane_rate = 13.50			
07: [7] Link Training test for lane count = 1 and lane_rate = 20.00			PASS
Number of emulated LTTPRs = 7			
<ul> <li>LTTPR mode = Non-Transparent Mode</li> </ul>			
<ul> <li>Link Training at 20.00Gbps and 1 lanes is successful.</li> </ul>			
> O8: [8] Link Training test for lane count = 2 and lane_rate = 20.00			
3 Q 09: [9] Link Training test for lane count = 4 and lane_rate = 20.00			PASS
pen ACA Data 07: [7] Link Training test for lane count = 1 and lane_rate = 20.00			

#### **DP 2.0 LTTPR Sink Compliance - Test Selection**

G DP 2.0 Source CT Core R1.0

	CDF Entry Test Selection Test Options / Preview		
elec	All 🛷 💥 Count Options	EXE	CUTE TEST
	TTPR		
>	4.9.1.1: [Draft in DP2.0] With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	4
>	4.9.1.2: [Draft in DP2.0] With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	4
>	4.9.1.3: [Draft in DP2.0] With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	4
5	4.9.1.4: [Draft in DP2.0] With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	4
>	4.9.1.5: [Draft in DP2.0] With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	1
5	4.9.1.6: [Draft in DP2.0] With 6 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	4
>	4.9.1.7: [Draft in DP2.0] With 7 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	1
5	4.9.1.8: [Draft in DP2.0]With 8 emulated LTTPR, Successful Link Training at all Supported Lane Counts and Link Speeds	1	1
3	4.9.1.9: [Draft in DP2.0] With random[1-8] number of emulated LTTPR, Successful Link Training at all Supported Lane Co	1	4
5	4.9.1.10: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training at all Supported Lane C	1	4
>	4.9.1.11: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training (Higher Differential Vo	1	4
>	4.9.1.12: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Link Rate/B	1	4
5	4.9.1.13: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Link Rate/B	1	4
5	4.9.1.14: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training (Higher Pre-emphasis	1	8
>	4.9.1.15: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training (Lower Link Rate/BW D	1	1
>	4.9.1.16: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training when EQ done at 20th	1	1
2	4.9.1.17: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth,	1	1
>	4.9.1.18: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth.	1	1
5	4.9.1.19: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth.	1	1
>	4.9.1.20: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth.	1	4
>	4.9.1.21: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth.	1	4
5	4.9.1.22: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth.	1	\$
÷.	4.9.1.23: [Draft in DP2.0]With random[1-8] number of emulated LTTPR, Successful Link Training to a Lower Bandwidth.	1	1

CLOSE

#### DP 2.0 LTTPR Device Compliance - Test Results

S DP 2.0 LTTPR Device CT Core R1.0	100	
Instrument: MyM41h [10.30.196.186] - Connect Cards		
CDF Entry Test Selection Test Options / Pr	eview	
Select All 💅 🗱 Count Options	Ð	
<ul> <li>Capability</li> </ul>		
> 7.1.1.1: [Draft in DP2.0]Data structure revision validation	1	4
> 7.1.1.2: [Draft in DP2.0]Phy repeater count validation	1	V
> 7.1.1.3: [Draft in DP2.0]Phy repeater lane count validation	1	1
> 7.1.1.4: [Draft in DP2.0]Phy repeater link rate validation	1	V
> 7.1.1.5: [Draft in DP2.0]Phy repeaters DPCD register validation at various LTTPR position.	1	V
> 7.1.1.6: [Draft in DP2.0]Phy repeater AUX read/write time budget validation	1	V
<ul> <li>8b10b-Transparent</li> </ul>		
> 7.1.2.1: [Draft in DP2.0]With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
> 7.1.2.2: [Draft in DP2.0]With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
> 7.1.2.3: [Draft in DP2.0]With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
> 7.1.2.4: [Draft in DP2.0]With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	V
> 7.1.2.5: [Draft in DP2.0]With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
> 7.1.2.6: [Draft in DP2.0]With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
> 7.1.2.7: [Draft in DP2.0]With 6 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	V
> 7.1.2.8: [Draft in DP2.0]With 7 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
✓ 8b10b-Non-Transparent		
> 7.1.3.1: [Draft in DP2.0]With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	V
7.1.3.2: [Draft in DP2.0]With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	V
7.1.3.3: [Draft in DP2.0]With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b		4
7.1.3.4: [Draft in DP2.0]With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	4
<ul> <li>7.1.3.5: [Draft in DP2.0]With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b</li> </ul>	Link 1	V
7.1.3.6: [Draft in DP2.0]With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b		4
7.1.3.7: [Draft in DP2.0]With 6 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b		V
7.1.3.8: [Draft in DP2.0]With 7 emulated LTTPR, Successful Link Training at all Supported Lane Counts and 8b10b	Link 1	1
<ul> <li>UHBR tests</li> </ul>		
7.1.4.1: [Draft in DP2.0]With 0 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		4
7.1.4.2: [Draft in DP2.0]With 1 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		4
7.1.4.3: [Draft in DP2.0]With 2 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		4
7.1.4.4: [Draft in DP2.0] With 3 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		4
7.1.4.5: [Draft in DP2.0] With 4 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		4
7.1.4.6: [Draft in DP2.0]With 5 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		V
7.1.4.7: [Draft in DP2.0]With 6 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR		V
> 7.1.4.8: [Draft in DP2.0]With 7 emulated LTTPR, Successful Link Training at all Supported Lane Counts and UHBR	Link 1	1
		-
		CLOSE

#### **DP Aux Channel Traces – From LTTPR Test**

Ope	n Clo	se Export	Options	Filter	Find					
		LO1 Events: 2674		ritter	ring					
DR DR	DNAT		+00132:37,8031		R:90 FEC CAPABILITY L-1			art Time: +00:32:37.865648		
19	DNAT		+00:32:37.803		ACK BP	1	30	Type: Native		
10	DNAT		+00:32:37.803		R:60 DSC SUPPORT L=16		D	irection: Reply		
11	DNAT		+00:32:37.803		ACK 01 21 03 7F FB 07 01 00 00 1F 0E EE			Command: ACK		
12	DNAT		+00:32:37.803		R:D eDP CONFIGURATION CAP L=1	Re	ply to	Read Request.		
13	DNAT		+00:32:37.8034		ACK DD	1.00				
14	DNAT		+00:32:37.803		R:701 EDF GENERAL CAPABILITY 1 L=1	10		NADO	Value	Description
15	DNAT		+00:32:37.803		KCK 87					
16	DNAT		+00:32:37.8038		1702 EDP BACKLIGHT ADJ CAPS L-1			Minor Revision Number	0	
17	DNAT		+00:32:37.8031		ACK 22		7-4	Major Revision Number	2	
18	DNAT		+00:32:37.8040		1725 EDF PWMGEN BIT COUNT MIN L=2	20	001: 8	b/10b MAX LINK RATE PHY REPEATER		
19	DNAT		+00:32:37.8040		ACK D2 OC		Bit	Nane		Description
20	DNAT		+00:32:37.8041		22E RX ALFM CAPABILITIES L=1					
21	DNAT	DPUSBC-R13	+00:32:37.8042		ACK 03		7-6	MAX_LINK_RATE	1Eh	8.1 Obps/lan
222	DNAT	DPUSBC-R13	+00:32:37.8043	308 >	116 RX ALPM CONFIGURATION L=1 01	8 70	002: P	HY REPEATER CNT		
923	DNAT	DPUSBC-R13	+00:32:37.804		VCK				Value	Description
924	DNAT	DPUSBC-R13	+00:32:37.8044	449 >	1:2214 FEATURE ENUMERATION LIST CONT L=1					
925	DNAT	DPUSBC-R13	+00:32:37.8045	523 <	ACK 01		7-0	LTTPR Count	01h	
926	DNAT	DPUSBC-R13	+00:32:37.8044	603 >	R:7 DOWN STREAM PORT COUNT L=1	70	003: P	BY REPEATER MODE		
927	DNAT	DPUSBC-R13	+00:32:37.8044		ACK 41		Bit	Nane	Value	Description
928	DNAT	DPUSBC-R13	+00:32:37.8047	745 >	R:7 DOWN STREAM FORT COUNT L=1			Mode		Transparent
929	DNAT	DPUSBC-R13	+00:32:37,8048	819 <	ACK 41		7-0	Mode	son	Transparent
930	DNAT	DPUSBC-R13	+00:32:37.804	902 >	. 10A eDP_CONFIGURATION_SET L=1 00	20	004: M	AX LANE COUNT PHY REPEATER		
931	DNAT	DFUSBC-R13	+00:32:37.8049	984 <	ACIK				Value	Description
932	DNAT	DPUSBC-R13	+00:32:37.8050	043 >	120 FEC_CONFIGURATION L=1 01		4-0	MAX LANE COUNT		Four lanes
933	DNAT	DPUSBC-R13	+00:32:37.805	125 <	NCK.		5	BRA DARE COURT		Reserved
934	DNAT	DPUSBC-R13	+00:32:37.805	186 >	R:201 DEVICE_SERVICE_IRQ_VECTOR L=1		6		0	Reserved
935	DNAT	DPUSBC-R13	+00:32:37.805	260 <	NCK DD		7		0	Reserved
936	DNAT	DPUSBC-R13	+00:32:37.865	430 >	R:E TRAINING AUX_RD_INTERVAL L=1	20	005- P	HY REPEATER EXTENDED WARE TIMEOR		
937	DNAT		+00:32:37.8655		ACK 81	10				Description
938	DNAT		+00:32:37.8655		A: PO000 LTTPR FIELD DATA STRUCTURE REV L-8					**********
939	DNAT	DPUSBC-R13	+00:32:37.865		ACK 20 1E 01 55 04 10 01 07		6-0	EXT WARE TIMEOUT REQUEST EXT WARE TIMEOUT GRANT	16 N(0)	
40	DNAT		+00:32:37.8658		*: POD03 PHY_REPEATER_MODE L=1 AA			DAT_MARE_TIMEOUT_GROAT	H(0)	
41	DNAT	DPUSBC-R13	+00:32:37.8658		NCK.	20	006: N	AIN LINK CHANNEL CODING PHY REPR	ATER	
42	DPLT	DFUSBC-R13	+00:32:37.867	795 >	(:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02		Bit	Nane	Value	Description
43	DPLT		+00:32:37.8678		ACK.			128b/132b SUPPORTED	Y(1)	
44	DPLT	DPUSBC-R13	+00:32:37.8675	935 >	#:100 LINE_BN_SET L-1 04		-	\$39: < ACE 20 1E 01 55 0		1.07

## PANEL REPLAY FUNCTIONAL TESTING

#### Panel Replay Testing

The M42d's supports functional testing of Panel Replaycapable source and display devices. The analysis support for testing sources provides emulation of a Panel Replay sink device. The Panel Replay sink functional test enables you to configure selected update regions through the command line (GUI implementation is future).

#### **Panel Replay Source Analysis**

The Real Time analyzer provides a real time update view (below) showing the incoming Panel Replay VSCs where you can see the changes from the previous frame. The transaction list (below right) shows the Panel Replay VSC metadata packets that have been sent with Selected Update regions. The panel on the right depicts the areas (blue box) where the selected transaction (left panel) VSCs and the SUs have indicated at change.

# Total: 449 VMete: 70.1 fps 182, 37 RGB sRGB, VESA 3 bpc Progres Frame/Field Sequential, type=8 VSC SDP supporting 3D stares = PR VSC peyload dues not o Do not update the RFB 01 03 04 05 06 07 08 09 10 11 12 13 14 15 16 18 19 20 21 22 23 24 25 26 27 26 29 38 31 06

#### Capture Analysis Showing VSCs

Data

CSB

5004

5005

5006

5007

5008

5009

5010

5011

5012

5013

5014

5015

5016

5017

5018

5019

#### DP VC Viewer Events/Data Frames panel-replay-capture [VC-1] Open Segment Rows Events Find Time: HH:MM:SS.ms.us.ns(r, r) ⑦ ⑦ ⑦ ● Q Marker 1: ● > Marker 2: ● > Time: HH:MM:SS.ms.us.ns(.ps) -549117 (0:0:0.003.389.611.111) 00000000 00000000 00000000 00000000 SS 0D110000 00000084 0000001B 00000048 00000000 00000000 00000000 00000000 -9 00000000 00000000 00000000 00000000 SE SE SE 00000000 00000000 00000000 00000000 00000000 00000000 00000000 0000000 -4 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 55 55 35 +0 01010000 06050007 10090006 14130010 469485 Link Clock # 17000403 25001211 • Valid Bytes: Stereo Method: Method Data: Link Clock TimeStamp Туре +2 00201918 00242322 00282726 00003130 1 (Frame/Field Sequential) 0:0:0.002.897.925.926 469464 SS SE SE SE 469465 0:0:0.002.897.932.099 Audio TimeStamp Active +4 00000000 0000000 00000000 0000000 PR STATE: 469468 0:0:0.002.897.950.617 SE CRC VALID: 00000000 00000000 00000000 00000000 469474 0:0:0.002.897.987.654 SS U COORDINATES VALID: Update the RFB 0x0403 00000000 00000000 00000000 0000000 for R/Cr: for G/Y: for B/Cb: 469475 0:0:0.002.897.993.827 CTA Audio 00000000 00000000 00000000 00000000 469478 0:0:0.002.898.012.346 SE +8 00000000 0000000 00000000 0000000 469484 0:0:0.002.898.049.383 ss +9 SS SS 88 Update Region X-Coord: Update Region Y-Coord: 4105 469485 0:0:0.002.898.055.556 VSC 00000000 0000000 00000005 00000013 Update Region Width: Update Region Height: 469488 0:0:0.002.898.074.074 SE 4625 00000000 00000000 00000000 0000000 469494 0:0:0.002.898.111.111 SS 5653 +12 00000081 00000000 00000000 00000000 469495 0:0:0.002.898.117.284 VSC SE SE SE 469498 0:0:0.002.898.135.802 SE 00000000 00000000 00000000 00000000 10 00 13 14 15 16 00 29 30 31 00 00 469877 0:0:0.002.900.475.309 BS 00000000 00000000 00000000 Lane 2: 06 00 09 10 11 12 00 25 26 27 28 00 Lane 1: 07 00 05 06 07 08 00 21 22 23 24 00 +15 00000000 469878 0:0:0.002.900.481.481 BS Data +16 00000000 00000000 00000000 00000000 470301 0:0:0.002.903.092.593 Lane 0: 00 00 01 01 03 04 00 17 18 19 20 00 00000000 00000000 00000000 00000000 470302 0:0:0.002.903.098.765 BS Data 00000000 00000000

#### Panel Replay Aux Channel Monitor

The M42d enables you to view the Aux transactions for discovery and configuration of Panel Replay (below).

			Export Options Filter Find CD6] Events: 12 (24)				
P 0 1 2 2 3 3 4 4 5 5 6 6 7 7 8 9 9 10 11	anelRep DNAT DNAT DNAT DNAT DNAT DNAT DNAT DNAT	13 13 11 11 11 13 13 11 11 11 13	CD0[cvmin12[24] 5 R:200 SING_COUNT L=8 4 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 4 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 4 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 4 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 4 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 4 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 R:200 SING_COUNT L=8 5 ACK 41 00 77 77 05 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 70 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 70 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 03 00 00 5 ACK 41 00 77 77 75 00 00 00 00 00 00 00 00 5 ACK 41 00 77 77 75 00 00 00 00 00 00 00 00 00 00 00 00 00		Description Reserved Reserved Reserved Reserved Reserved Reserved		
			[0000][00 03][	1			

#### **Capture Analysis**

You can capture the Panel Replay VSC metadata packets in the Capture Analyzer (bottom) where you can examine the VSCs showing the Selected Update (SU) regions per captured frame.

#### **Receiver – Analyzer Transaction List**

A64														
Set EDID			DP										RX Mode: Emu	lation 💌
Tools Passive Monitor	ES UNKR				Default 6 b	pc 64	배이다 0x480p@60Hz		RIZONTAL I 50kHz		CHANNELS 2 SAMPLE RATE 48 kHz			INK RATE 10.00Gbps
	inel Repl	lay												
	Clear	Stop	Open s	Save As	Option	IS	Fra	me Panel On		Scale (H:V)	• x -	у [	+ ]	
	<real-< th=""><th>Time&gt;</th><th></th><th></th><th></th><th></th><th></th><th></th><th>8</th><th></th><th></th><th></th><th></th><th></th></real-<>	Time>							8					
	619	Frame 1165/	Line	PR	SU Inval	X.Y U,60	W,H 40,30	Frame W, 640,480	н					
	620	11657	2	ON	Inval	0,60	40,30	640,480						
	621	11662	165	ON	Inval	40,90	40,30	640,480						
	622	11663	2	ON	Inval	40,90	40,30	640,480						
	623	11663	2	ON	Inval	40,90	40,30	640,480		11				
	624	11668	165	ON	Inval	80,90	40,30	640,480						
nel Repl	625	11669	2	ON	inval	80,90	40,30	640,480						
DIF/Tri_	626	11669	2	ON	Inval	80,90	40,30	640,480						
	627	11674	165	ON	Inval_	120,90	40,30	640,480						
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#### **DisplayPort 2.0 Capabilities**

Version	DisplayPort 2.0 (and DP 1.4)
Standard Video Formats	VESA, CTA
Protocols and Line Coding	DP, DSC, FEC, MST, SSC, SDP with 128b/132b encoding (LTTPR, Panel Replay)
Video Data Rates	1.62, 2.7, 5.4, 8.1, 10.0, 13.5 & 20 Gb/s; 1, 2, 4 Lanes
Video Encoding / Color Depths	RGB, YCbCr - 8, 10, 12, 16 bits (6 bits future)
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0
HDCP	Versions 1.3 and 2.3
Audio	8 Channel LPCM programmable sine wave
Capture memory	8 GBytes

#### **Connectors - Front**

DP Standard	Tx (1) DP Full-Sized; Rx (1) DP Full-Sized
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
eDP Header	Pins to access eDP Tx backlight controls
USB (2)	For connecting keyboard and mouse for ATP Manager control & external storage media

#### Connectors – Back

HDMI - Admin Connector	HDMI 2.0 Port for external monitor for ATP Manager GUI
USB (2); USB-C (2)	Keyboard / mouse connected to USB ports to control ATP Manager on external display connected to Admin HDMI 2.0 port
RJ45 E1	For admin control over LAN from computer running ATP Manager
Cross Sync connector	Use for triggering a capture or for a capture event to trigger an oscilloscope (future)
All other connectors	Not used

#### Physical/Electric/Admin

Power	100-240 VAC, 50-60 Hz, 200 Watts
Size / Weight	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm) - 7.6 LBS; 5.057 Kg
Rack mountable	2 RU mounts in 19-inch rack with rack mounting brackets
Internal speaker	Speaker with volume control for monitoring incoming LPCM audio (future)
Command Line Control	Ethernet (RJ-45) for external GUI
System Control	External PC connected over LAN to Ethernet RJ45, VNC or Keyboard/mouse and 4K TV at Admin HDMI port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

Ordering/Product Code Description 00-00259 M42d UHBR Video Analyzer/Generator (This is the Hardware System with basic video generation and analysis) 00-00261 M42d HBR3 Video Analyzer/Generator (This is the Hardware System with basic video generation and analysis) 95-00221 M42d Upgrade from HBR3 00-00261 System to UHBR rates with 00-00259 System 95-00222 Passive Probing Main Link and Aux Channel Sink Enhanced Functional test - Includes DSC, LTTPR, Panel Replay & Adaptive Sync Functional Tests 95-00225 Source Enhanced Functional test - Includes DSC, Capture Analysis, LTTPR, Panel Replay, Adaptive Sync Functional 95-00226 DP 1.4 Sink EDID/DisplayID compliance tests (requires 95-00225) 95-00227 95-00228 DP 1.4 Source EDID/DisplayID compliance tests (requires 95-00226) DP 1.4/2.0 Source Link Layer & (MST future) compliance tests 95-00232 (DP 2.0 tests not fully supported; full suite future) (requires 95-00226) DP 1.4/2.0 Sink Link Layer & (MST future) compliance tests 95-00233 (Limited DP 2.0 tests currently supported; full suite future) (requires 95-00225) DP 1.4/2.0 DSC/FEC Source compliance tests (DP 2.0 tests are future) (requires 95-00226) 95-00236 95-00237 DP 1.4/2.0 DSC/FEC Sink compliance tests (DP 2.0 tests are future) (requires 95-00225) 95-00240 NEW! DP 1.4/2.0 LTTPR Source compliance tests (requires 95-00226) DP 1.4/2.0 LTTPR Sink compliance tests (requires 95-00225) 95-00241 NEW! 95-00242 NEW! DP 1.4/2.0 LTTPR Device compliance tests (requires 95-00225 & 95-00226) 95-00234 DP 1.4/2.0 Adaptive Sync Source compliance test (support for DP 2.0 UHBR rates is future) (requires 95-00226) 95-00235 DP 1.4/2.0 Adaptive Sync Sink compliance test (support for DP 2.0 UHBR rates is future) (requires 95-00225) 95-00214 HDCP 2.3 Source compliance tests (requires 95-00226) 95-00217 HDCP 2.3 Sink compliance tests (requires 95-00225) 95-00212 Embedded DisplayPort (eDP) (Limited functions supported) M41x Rack-mount Kit



95-00209





#### 绿测科技有限公司

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