

# quantumdata™ M41h

## 48G Video Analyzer/Generator for HDMI Testing

### Deep Analysis & Generation of HDMI 2.1 Fixed Rate Link (FRL) w/ Forward Error Correction (FEC)

### Entry Level Tester Upgradable to Full Compliance



#### Key Features

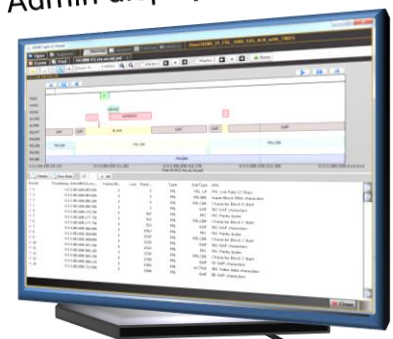
- Verify the 16b/18b encoding for Fixed Rate Link (FRL) Packets in both 3 and 4 lane configurations
- Use generator or analyzer in three (3) Lane configuration mode at 3Gbps & 6Gbps data rates and four (4) Lane configurations at 6Gbps through 12Gbps (48Gbps aggregate)
- Video generator function supports TMDS and FRL for video resolutions up to 8K at 2376MHz pixel rates
- Certified "Test Device Approved for Dolby Labs, Inc." for HDMI & eARC Dolby audio generation & analysis including Source Led Dolby Vision tests.
- Evaluate 4K & 8K HDR10 UHD TVs w/HDR Lab
- View captured FRL and TMDS data elements graphically in Event Plot and in Data Decode table; use searching and filtering to find data
- View FRL packet mapping into Character Blocks and Character Block mapping into Super Blocks
- Verify Display Stream Compression (DSC) on FRL, DSC capable source or sink devices.
- Run FRL & DSC source & sink compliance tests
- Run eARC the full suite of compliance tests on an eARC Tx or Rx device
- Run TMDS source & sink compliance tests
- Run HDCP 2.3 source, sink & repeater compliance tests
- View TMDS video, protocol, data island, preamble and control elements
- Monitor of FRL Link Training transactions in the Auxiliary Channel Analyzer utility to show SCDC reads and writes over the DDC channel
- Run pixel error test on incoming TMDS
- Passively monitor DDC channel in TMDS or FRL mode (FRL mode requires custom cable)
- Passively monitor the TMDS Video and metadata (without HDCP) and DDC channel between a source and sink
- View Lane Error Counts and Reed Solomon Corrections Count in the SCDC CED registers
- Verify the eARC common mode channel on either an eARC Tx or Rx device
- **NEW!** Test sinks with QMS-VRR
- **NEW!** Run HDR10+ Source Side Tone Mapping (SSTM) tests on UHD TVs
- **NEW!** Tests Power Cable Assemblies (PCA) for power requests
- Run test automation for compliance tests with the API

The Teledyne LeCroy quantumdata M41h 48Gbps Video Analyzer / Generator for HDMI Testing is a compact, versatile test instrument that can be easily extended from an entry level functional tester to a full certified compliance tester. The M41h is equipped with both HDMI Tx and Rx ports supporting HDMI 2.1 Fixed Rate Link and FEC capture analysis and decode up to 48Gbps (12Gbps/Lane). The HDMI Rx analyzer port provides visibility into the Fixed Rate Link packetization—super blocks, character blocks and FRL packets and underlying TMDS video, protocol, control and metadata elements. The HDMI Tx video generator port transmits Fixed Rate Link video streams with embedded TMDS video, protocol, control and metadata elements. The M41h also supports the full suite of FRL source and sink compliance tests as well as Enhanced Audio Return Channel (eARC) compliance testing for both Tx and Rx devices. An extensive Application Programming Interface (API) is supported for automated testing systems available thru a command line interface.

#### Operation

The M41h supports video generation and analysis of the FRL/FEC HDMI data streams through the user-friendly GUI Manager which presents the data in an easy to understand way. The GUI can be controlled either via a laptop connected to the M41h or through a USB keyboard and mouse and a connected UHD HDMI admin display.

Admin display for ATP Mgr



#### M41h 48Gbps Video Analyzer / Generator

Keyboard & mouse for ATP Manager control

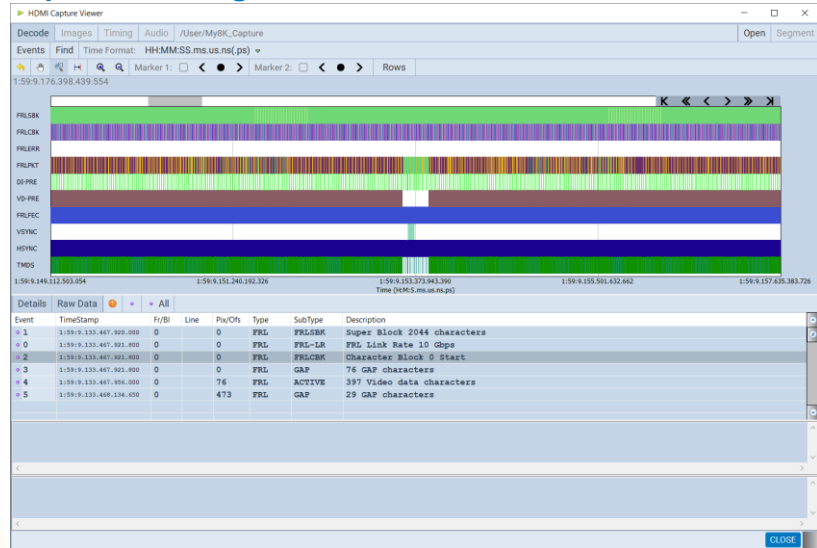


# FIXED RATE LINK (FRL) ANALYSIS

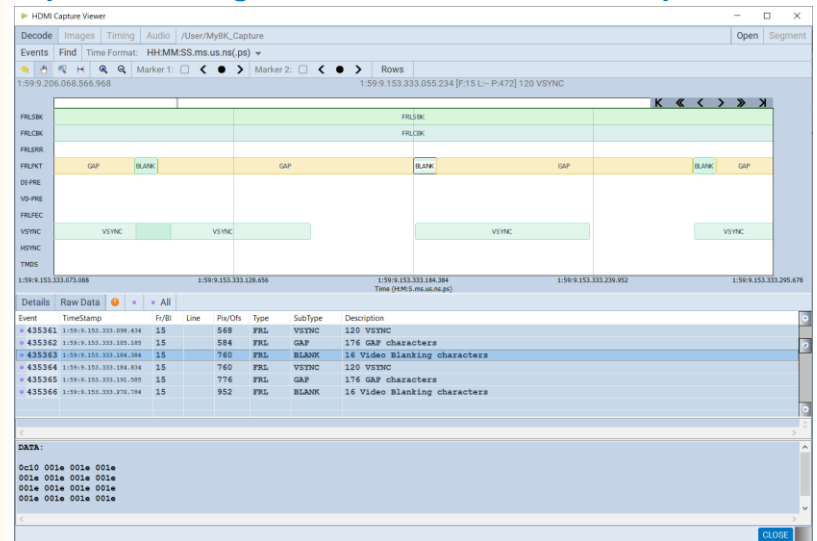
## Capture and Decode (FRL & FEC)

The M41h analyzer captures and decodes incoming HDMI 2.1 streams (HDCP encrypted or unencrypted) that have been packetized with FRL packet structures. These FRL data elements are depicted graphically in the Event Plot. The decoded data is shown in table form in the Data Decode window. The Forward Error Correction (FEC) characters are also shown as well. The module reports the Lane Error Counts and the FEC Reed Solomon Corrections Count in the SCDC registers. The underlying tri-byte video and protocol elements, e.g. active video, data island and preamble blocks, are also depicted and decoded. Each element is assigned a precise time stamp. Users can search and filter the FRL captured data by type.

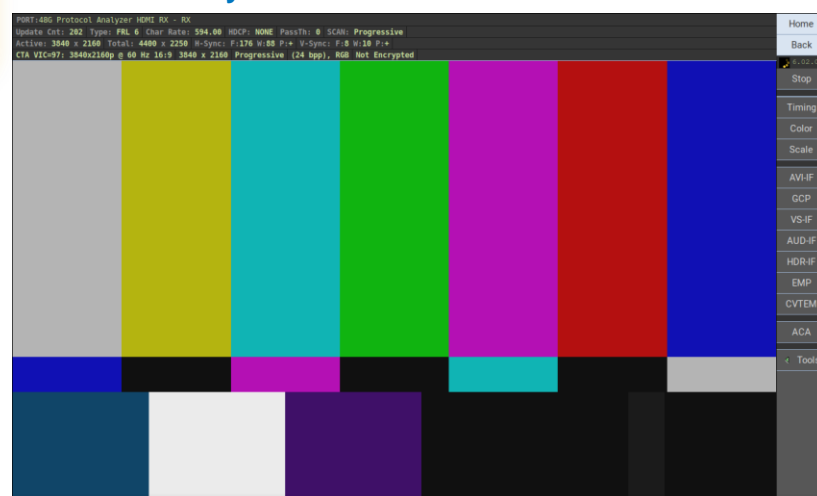
## Capture Showing SCDC, FRL & TMDs Elements



## Capture Showing FRL Packets, Character & Super Blocks



## Real Time Analysis



Admin Display for M41h GUI

HDMI 2.1 FRL-Capable Source DUT

M41h

Test Setup for Source Test

## Real Time Analysis

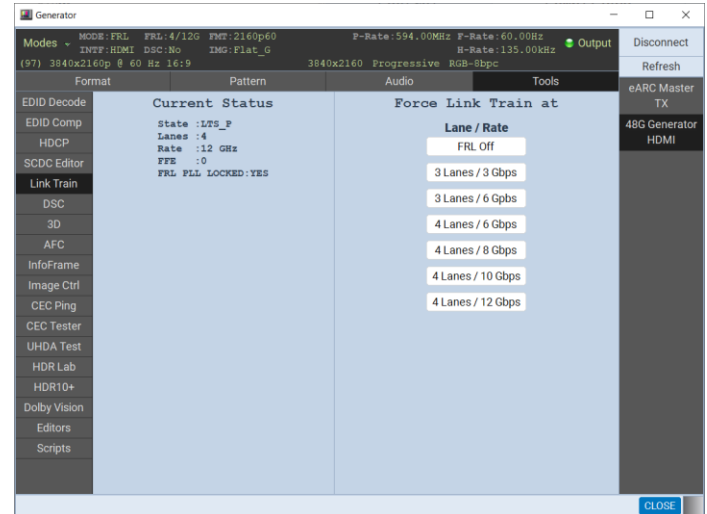
The M41h's Real Time analysis feature enables you to monitor the incoming TMDs and FRL video and metadata, data islands and InfoFrames including High Dynamic Range (HDR) InfoFrames. A status bar at the top of the window provides an at-a-glance view of the essential incoming video parameters.

# FIXED RATE LINK (FRL) LINK TRAINING ANALYSIS

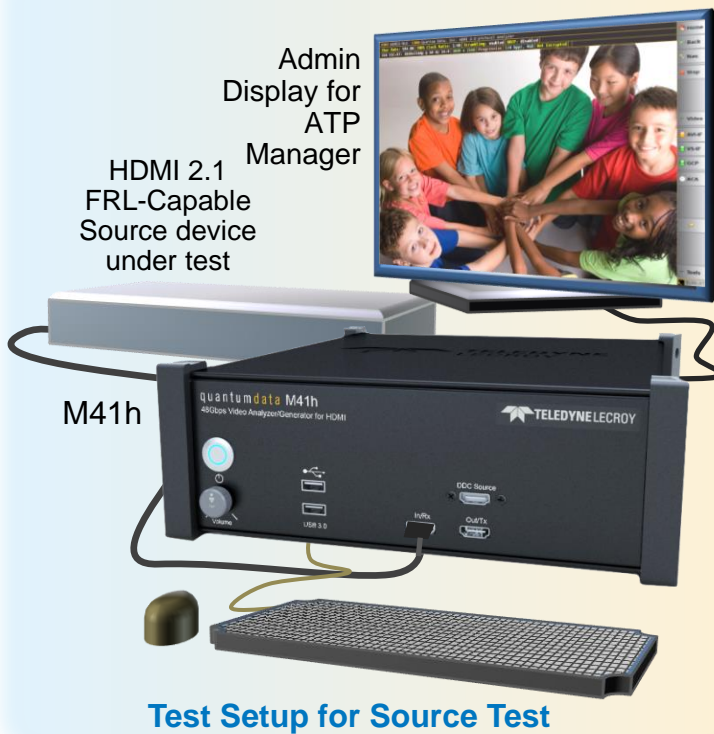
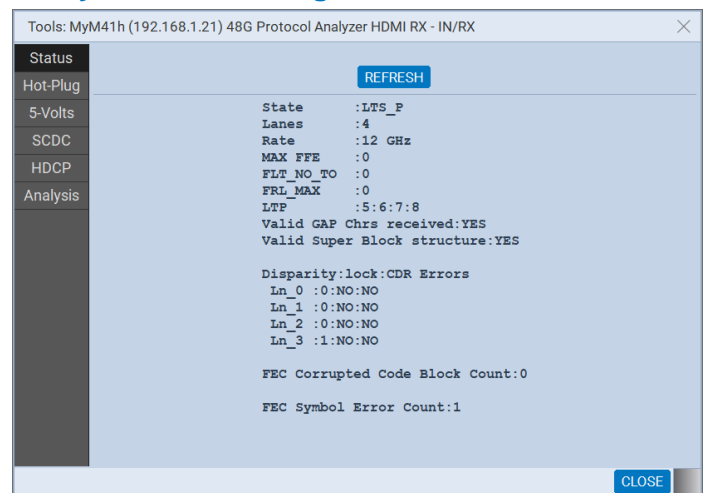
## Link Training

The M41h supports Link Training configuration and control. The module emulates an HDMI 2.1 sink indicating the max FRL rate in the HF-VSDB of the EDID and various other essential link training parameters in the SCDC control registers.

## Generator Link Training Status & Control Screen



## Analyzer Link Training Status Screen

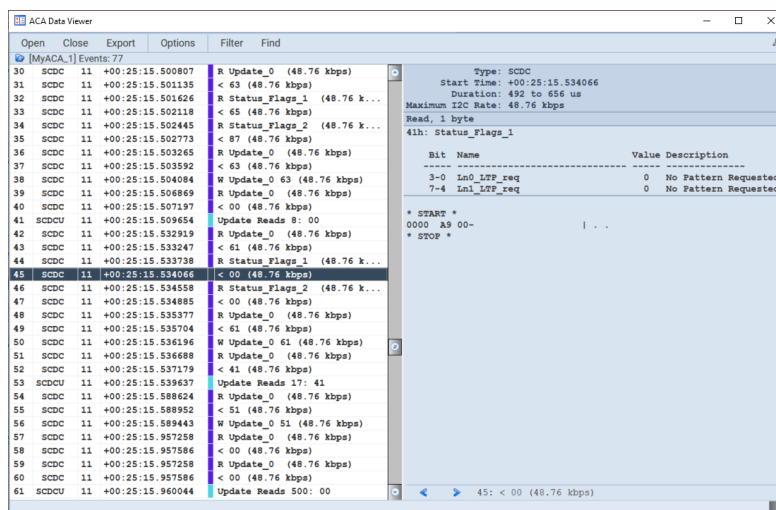


## Test Setup for Source Test

## Auxiliary Channel Analyzer

You can use the M41h to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel—with the Aux Channel Analyzer (ACA) utility. This enables you to verify link training functions to identify potential interoperability problems.

## Auxiliary Channel Analyzer (Link Training over DDC)





# FIXED RATE LINK (FRL) VIDEO GENERATION

## FRL Video Generation

The M41h for HDMI Testing enables developers of HDMI and TMDS FRL-capable sink devices and silicon makers to run functional tests on their FRL-capable display devices by rendering uncompressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s and up to pixel rates of 1485MHz. The enhanced video generator function enables specific selections of video formats, colorimetry, bit depth, chroma subsampling, color space and test patterns.



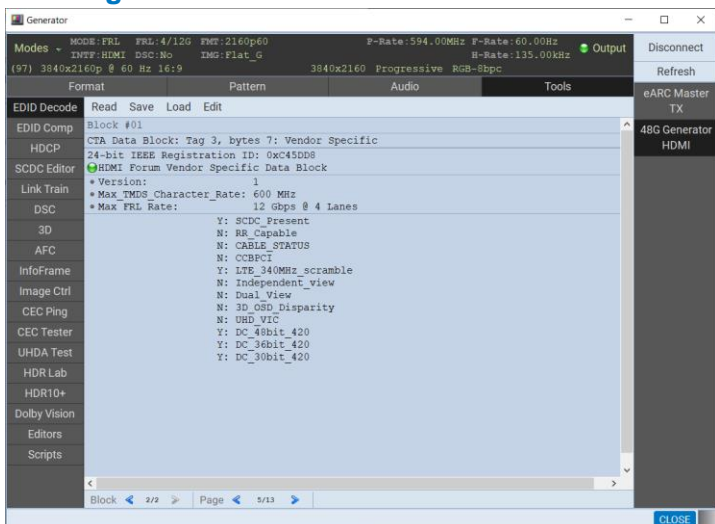
## Link Training Configuration

The M41h's video generation function enables you to configure the lane rate and number of lanes for transmission of the FRL stream.

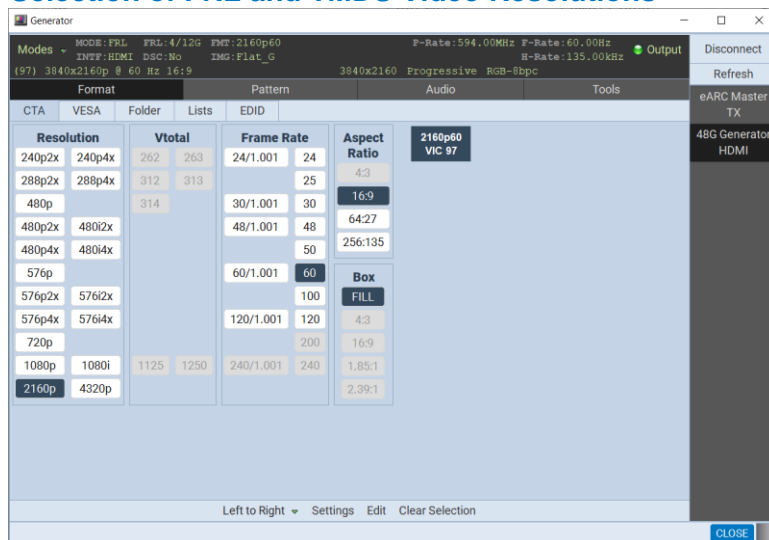
### EDID Read

The M41h enables you to view the EDID of the connected display (below). You can page through each block and save for later viewing.

### Reading the EDID



## Selection of FRL and TMDS Video Resolutions



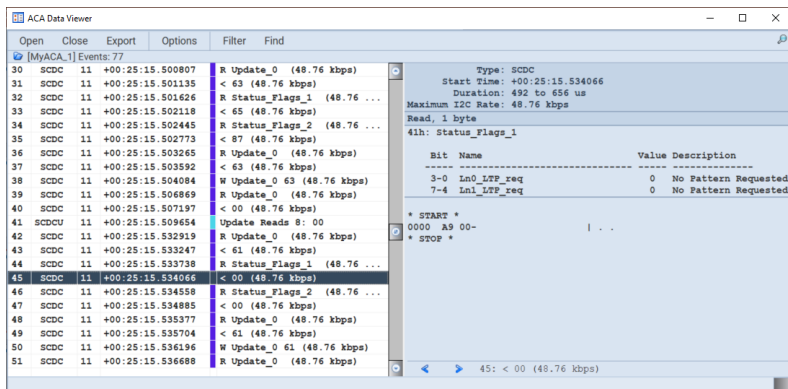
## Link Training Configuration



## Auxiliary Channel Analyzer (ACA)

You can use the M41h to monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel—with the Aux Channel Analyzer utility. The FRL link training transactions enable developers to verify that their displays are properly conducting their role in the link training process.

## Auxiliary Channel Analyzer (Link Training)



# HDR FUNCTIONAL TESTING – HDR LAB, DOLBY VISION, HLG

## HDR Lab UPDATES

The “HDR Lab” test option was developed jointly with industry expert Joe Kane. HDR Lab is a suite of 4K and 8K test patterns and reference images for evaluating HDR10 displays (examples at right) that address the following:

- HDR End-to-End Validation in Post Production – Verifies HDR metadata, color grading and color decoding throughout the post production process.
- HDR Display Test Suite – Verifies various HDR attributes such as: peak brightness, native contrast, average brightness level, signal clipping, and color gamut on an HDR-capable UHD TV using a variety of test patterns.

**980 with 48G Protocol Generator module for HDMI Testing**

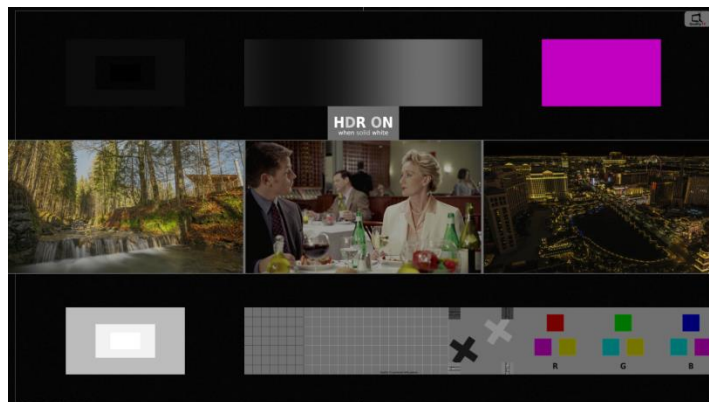


**HDMI UHD TV**

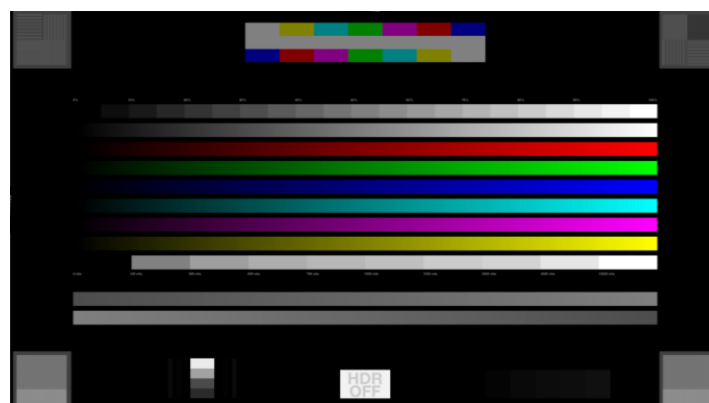


**Setup for HDR Functional Tests**

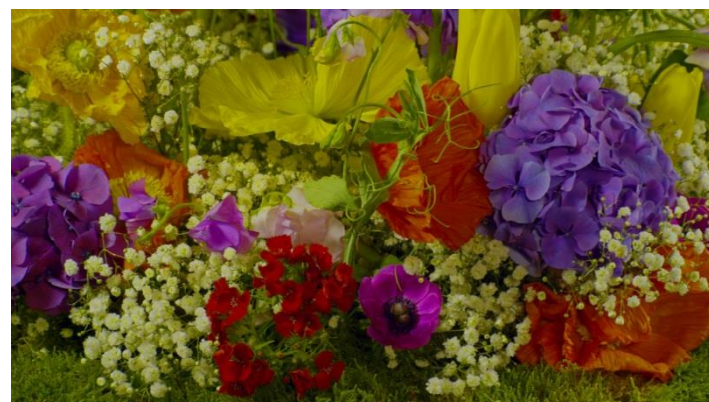
## HDR Lab (Sample Test Pattern - Combination)



## HDR Lab (Sample – Universal Test Pattern)



## HDR Lab (Sample Test Pattern – Flower Montage)



## Dolby Vision & Hybrid Log Gamma Test Pattern

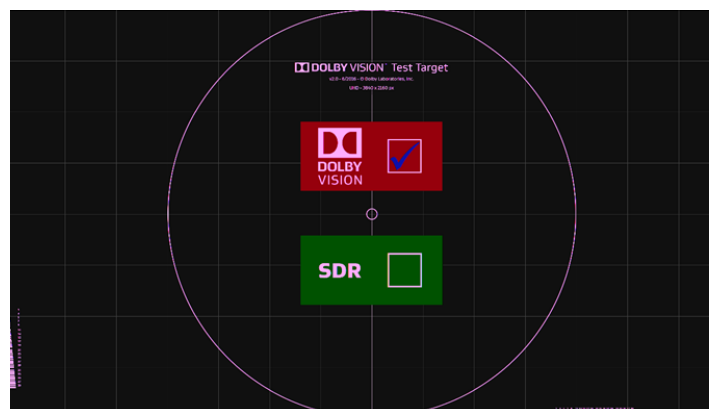
The Dolby Vision test image verifies a Dolby Vision display's Dolby Vision-specific EDID data, its response to the Dolby Vision protocol handshake and its handling of the Dolby Vision signal and metadata. The Dolby Vision test image will be rendered with a checkmark in the proper location if the display has properly interpreted the color space, metadata and checksum correctly.

The Hybrid Log Gamma (HLG) test image provides an assurance that the HLG metadata is not impeding the ability of the display to render the image.

## HLG Test Image



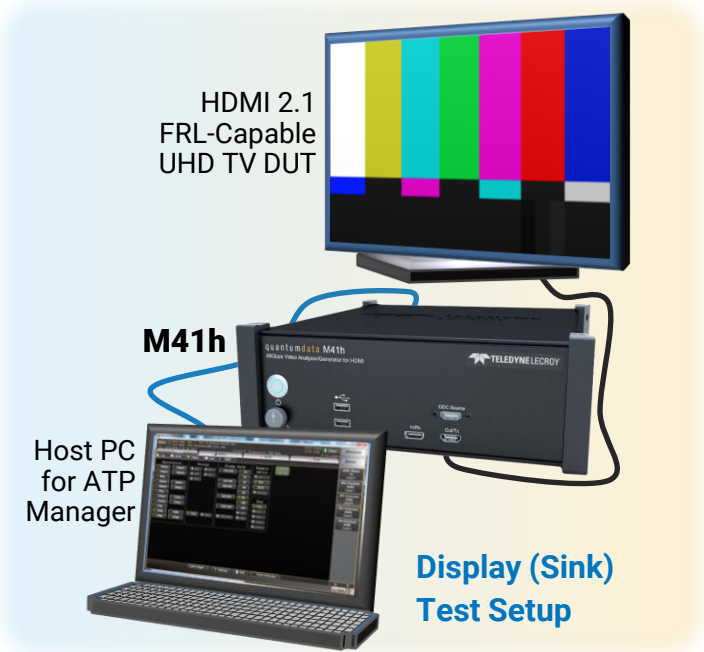
## Dolby Vision Test Image



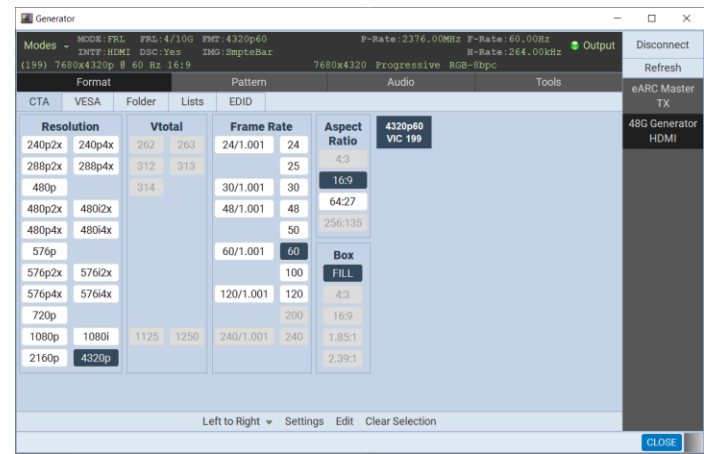
# DISPLAY STREAM COMPRESSION (DSC) TESTING

## DSC Video Generation

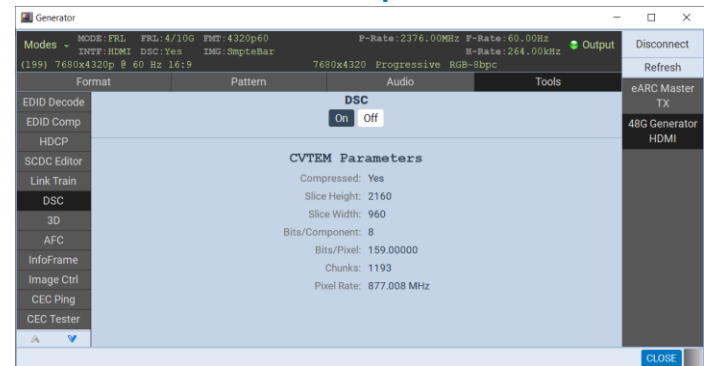
The M41h for HDMI Testing enables developers of HDMI DSC-capable sink devices and silicon makers to run Display Stream Compression (DSC) functional and compliance tests on their FRL-capable display devices by rendering compressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s. **NEW!** The test patterns and formats necessary to run the DSC sink compliance tests are pre-cached for fast rendering.



## DSC Video Generation Selection



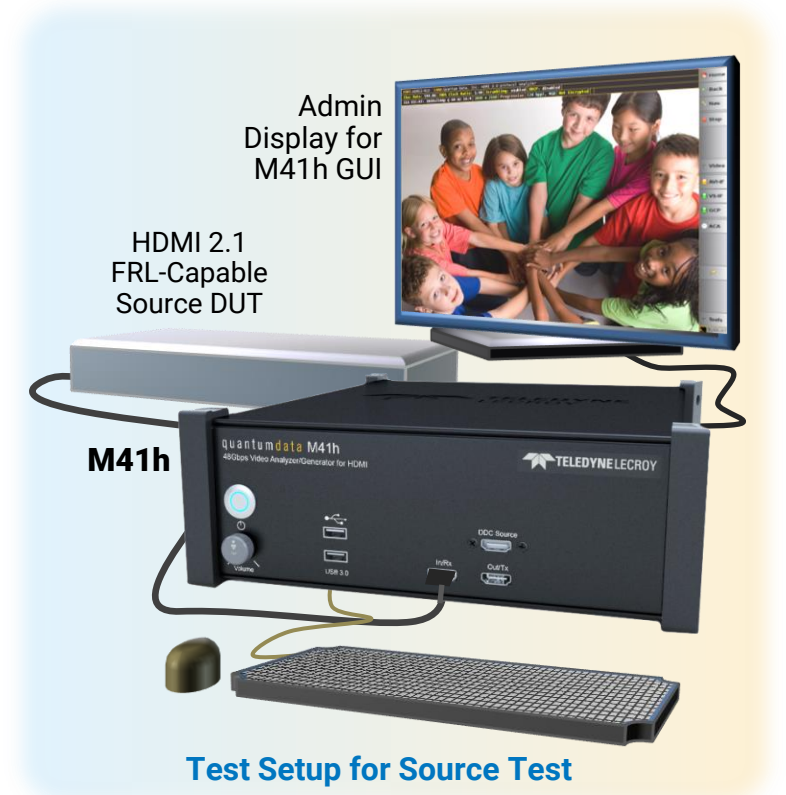
## DSC Video Generation Setup



## Display Stream Compression Video Analysis

The M41h for HDMI Testing enables developers of HDMI DSC-capable source devices and silicon makers to run Display Stream Compression (DSC) functional and compliance tests on their FRL-capable source devices by rendering compressed, unencrypted or encrypted FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s. **NEW!** There is a new "No Video" mode that enables you quickly verify the incoming DSC timing and metadata. You can then choose to view the uncompressed video frames.

## DSC Real Time Analysis







# FIXED RATE LINK (FRL) & DSC SINK COMPLIANCE

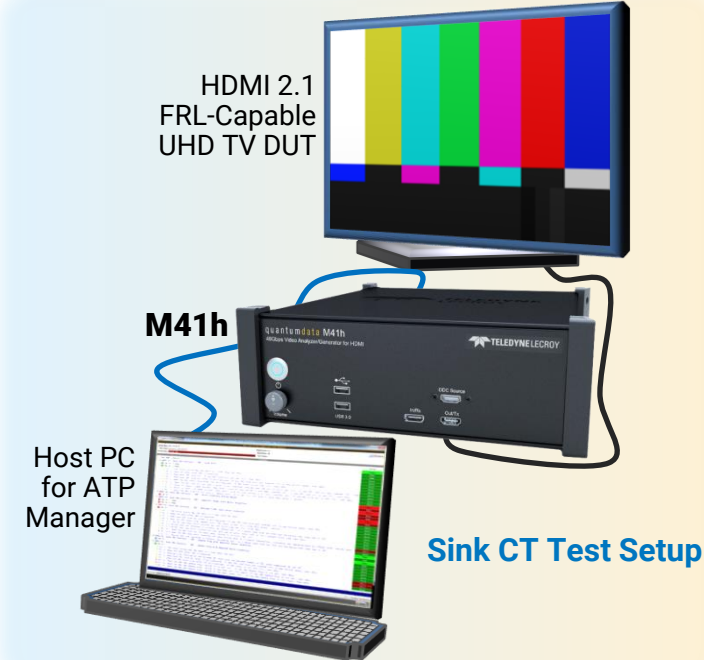
## FRL & NEW! DSC Sink Compliance Testing

The M41h for HDMI Testing enables developers of HDMI FRL and **NEW!** DSC-capable sink devices and silicon makers to run compliance tests on their FRL-capable sink devices with FRL streams at up to 8K video resolutions at lane rates up to 12Gb/s and at an aggregate link rate of 48Gb/s and pixel rates up to 1485MHz. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts. **NEW!** The test patterns and formats necessary to run the DSC sink compliance tests are pre-cached for fast rendering.

## Selection of FRL Sink & NEW! DSC Compliance tests

FRL Source			
Instrument: MyM41h [192.168.1.21]		Connect	Cards
CDF Entry		Test Selection	Test Options / Preview
Select All <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> Duration Options			EXECUTE TESTS
▼ Protocol			
▼	HFR1-11: Source FRL Protocol - Legal Codes		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-19: Source FRL Packets - FRL Map Characters		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-20: Source FRL Packets - FRL Control Periods		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-21: Source FRL Packets - Active Video FRL Packets (Uncompressed)		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-23: Source FRL Protocol - Data Flow Metering Variations		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼ Link Training			
▼	HFR1-10: Source FRL Protocol - FRL Link Training Patterns		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-12: Source FRL Protocol - Successful FRL Link Training		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-13: Source FRL Protocol - FRL Link Training - Link Rate Change		✓
	Iter 01: Source_Max_FRL_Rate < 2: Automatic PASS(SKIP)	--	✓
▼	HFR1-17: Source FRL Protocol - FRL Link Training - Future Rate Support		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼ 8bpc Encoding			
▼	HFR1-29: Source Pixel Encoding (FRL Mode) - RGB		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-30: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:2/4:4:4		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓
▼	HFR1-31: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:0		✓
	Iter 01: Source_Max_FRL_Rate = 0: Automatic PASS(SKIP)	--	✓

CLOSE



## NEW! Sample DSC Sink Compliance Test Results

Compliance Test Results Viewer

FRL Sink Compliance Test Results

HTML Report Instrument: MyM41h[10.30.196.32]

CONTINUE TEST EXECUTION

Results Name: MyDSC\_VICI196Test2

Manufacturer: Acme

Date Tested: June 29, 2020 6:00 PM

Model Name: XYZ

Overall Status: Incomplete

Port Tested: 1

Iter 05: (196) 7680x4320p @ 30 Hz 16:9, RGB, 10 bpc

Step 2.1, 2.2: Format is in the EDID and CDF

Step 2.3: CDF field Sink\_Supports\_DSC matches the DSC\_1p2 EDID field

Step 2.4: CDF field Sink\_DSC\_10bpc matches the DSC\_10bpc EDID field

Step 2.4: CDF field Sink\_DSC\_12bpc matches the DSC\_12bpc EDID field

Step 2.5: DSC\_10bpc field in the EDID is not set (=0)

Step 2.6: CDF field Sink\_DSC\_Native\_420 matches the DSC\_Native\_420 EDID field

01: 6 Gbps @ 3 Lanes, MIN Pixel Clock

02: 6 Gbps @ 3 Lanes, MAX Pixel Clock

Manual inspection of the DUT indicated inadequate support of the test signal.

03: 12 Gbps @ 4 Lanes, MIN Pixel Clock

04: 12 Gbps @ 4 Lanes, MAX Pixel Clock

Manual inspection of the DUT verified adequate support of the test signal.

Iter 06: (196) 7680x4320p @ 30 Hz 16:9, RGB, 12 bpc

Step 2.1, 2.2: Format is in the EDID and CDF

Step 2.3: CDF field Sink\_Supports\_DSC matches the DSC\_1p2 EDID field

Step 2.4: CDF field Sink\_DSC\_10bpc matches the DSC\_10bpc EDID field

Step 2.4: CDF field Sink\_DSC\_12bpc matches the DSC\_12bpc EDID field

Step 2.5: DSC\_10bpc field in the EDID is not set (=0)

Step 2.6: CDF field Sink\_DSC\_Native\_420 matches the DSC\_Native\_420 EDID field

01: 6 Gbps @ 3 Lanes, MIN Pixel Clock

Iter 06: (196) 7680x4320p @ 30 Hz 16:9, RGB, 12 bpc

–

1

FAIL

PASS

FAIL

PASS

PASS

PASS

–

1

PASS

PASS

CLOSE

## Sample Test Results of FRL Sink Compliance tests

Compliance Test Results Viewer

Results Name: NIK\_RS\_48\_Full

Date Tested: December 11, 2018 11:04 AM

Overall Status: ETS 2.1b - Fail

FRL Sink (2.1b) Compliance Test Results

Manufacturer: qd

Model Name: 980

Port Tested: 1

Test Results

Test Name / Details

HFR2-48: Sink FRL Protocol - RS - Basic Operation

Iter 01: 3 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 4. Read the RS\_C, verify that RS\_C Valid flag = 0; otherwise FAIL.

03: 7. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all active Lanes, else FAIL after 10 milliseconds

04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 10. Read the RS\_C, verify that RS\_C Valid flag = 1 and count = 0 or 1; otherwise FAIL

06: 11. Corrupt symbols at a rate of about 1e-9, spaced out over 10 seconds, with 1

07: 12. Read the RS\_C; if the value is not correct within 1 count then FAIL.

08: 13. Read the RS\_C again after 100 milliseconds; if the count is not 0 or 1 then

09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds, with 2

10: 15. Read the RS\_C; if the value is not correct within 1 count then FAIL.

11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating the

12: 17. Change the FRL data stream to be random data on all Lanes.

13: 18. After 5 seconds, read each FRL Lock bit and verify that they have all been

14: 19. Read the RS\_C, verify that RS\_C Valid flag = 1; otherwise FAIL

15: 20. If the count in the RS\_C is less than 4, then FAIL.

Iter 02: 4 Lanes

HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL

03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all a

04: 7. Read the RS\_C, verify that RS\_C Valid flag = 1 and count = 0 or 1; otherwise F

05: 8. Corrupt one symbol in each of a known random number (between 10000 and 30000)

06: 9. 100 milliseconds after the start of the symbol error, read the RS\_C and add

07: 11.1. If the correction count is outside the range of 12 from the number of gen

HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count

Iter 01:

HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count

HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL

03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all a

04: 7. Read the RS\_C, verify that RS\_C Valid flag = 1 and count = 0 or 1; otherwise F

05: 8. Write a 1 to the RS\_C Update flag to reset the flag.

06: 10. Corrupt one symbol in each of 32768 RS blocks over a 1-40second period at r

07: 11. Read the RS\_C RS\_C Update flag, verify that it has been set to a 1.

08: 13. Read the RS\_C RS\_C Update flag, verify that it is cleared to 0.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL CED Update flag, verify it is set (=1). If the CED Update flag is not set, then FAIL.

07: 14. Read the FRL CED Update flag, verify it has been set (=1) again. If the CED Update flag is not set, then FAIL.

08: 15. Read the FRL CED Update flag, verify it has been clear (=0). If the CED Update flag is not clear, then FAIL.

Instrument: S00000 [10.30.196.30]

Test Results

Test Name / Details

HFR2-17: Sink FRL Protocol - CED - Lock Bits

Iter 01: 3 Lanes

Iter 02: 4 Lanes

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.

04: 7. Read each FRL Lock bit after 100 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 8. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL

07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

08: 15. After at least 100 Super Blocks, read Lane 0 Lock bit and verify it is still cleared (=0). If the FRL Lock bit is set (=1), then FAIL.

09: 17. Read the FRL Lock bit for Lane 0. Repeat until it is set (=1) for Lane 0, else FAIL after 1 second.

HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads

Iter 01:

HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection

Iter 01: 3 Lanes

Iter 02: 4 Lanes

HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 5. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

04: 6. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 1 second

05: 8.1. Verify that each Error Counter has the Valid flag set (=1), else FAIL.

06: 8.2 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

07: 8.3 Verify that the Error Counter for any lane has an error count that is not 9 except first time then fail.

08: 10.1 Read the FRL Lock bit for each Lane, verify it is still set (=1).

09: 10.2 Read the FRL Lane Error Counter for each active Lane in a single transaction, including the checksum byte at offset 0x56. Verify that,

10: 10.3 Verify that the Checksum is correct, by adding the 7 or 9 bytes read from the SCDC and verifying that they sum to 0x0.

HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection

Iter 01:

HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection

Iter 01:

01: 1. CDF field Source Max FRL Rate is 0 then skip the test.

02: 3. Read the EDID after HPO is asserted.

03: 4. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the DUT.

04: 6. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.

05: 7. Read the FRL Start flag after 200 milliseconds. If FRL Start is not set (=1), then FAIL

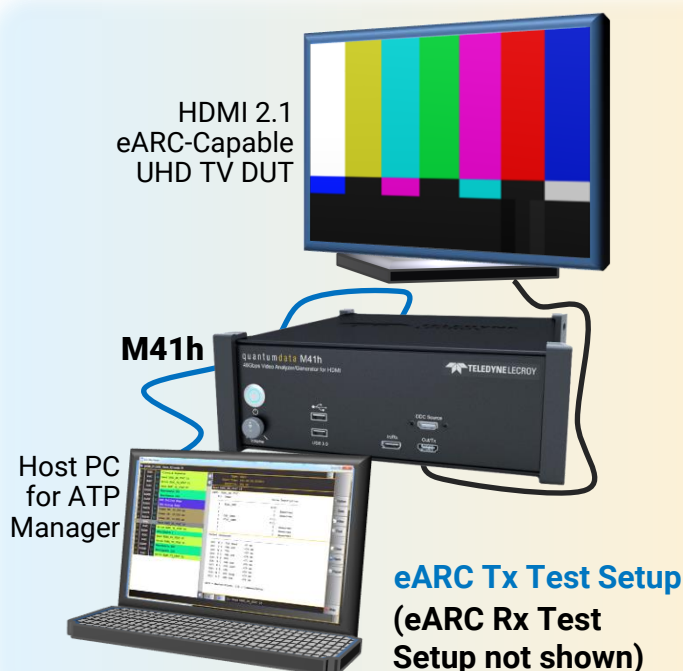
06: 11. Read the FRL CED Update flag, verify it is set (=



# eARC FUNCTIONAL AND COMPLIANCE TESTING

## eARC Functional Testing

The 48G Video Analyzer / Generator is also supports enhanced Audio Return Channel (eARC) Tx/Rx functional testing. The solution provides emulation of an eARC Tx and Rx functions over the eARC Common Mode and Differential mode data channels. Solution supports discovery and disconnect, heartbeat, status and capabilities data structure and transmission over the differential channel. (Sample screen showing monitoring incoming audio stream, right.)

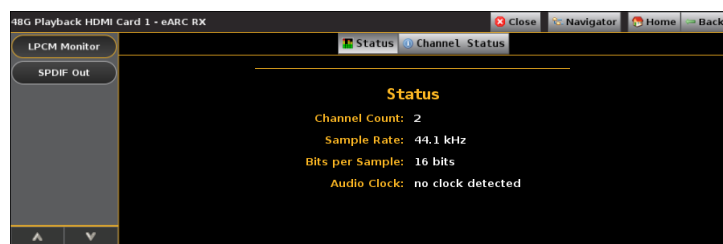
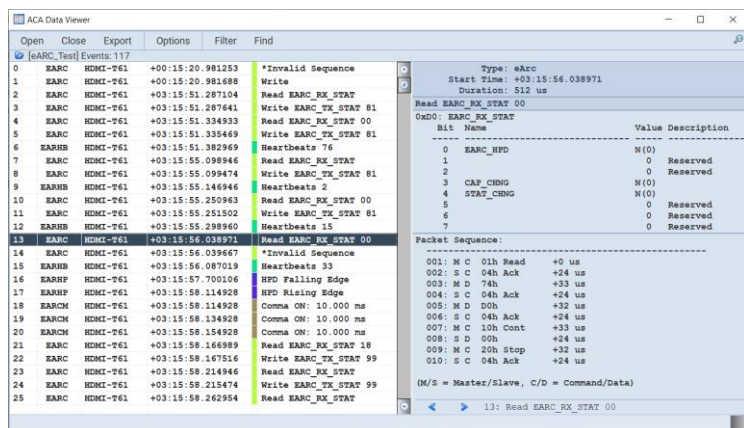


**eARC Tx Test Setup**  
(eARC Rx Test Setup not shown)

## Auxiliary Channel Analyzer (ACA)

The M41h can monitor the Link Training transactions—EDID exchange and reads and writes to the SCDC registers over the DDC channel -with the Aux Channel Analyzer (ACA) utility. Viewing the FRL link training transactions enables developers to verify their displays are properly conducting the link training process properly.

## Aux Chan Analyzer Traces (Common Mode Discovery)



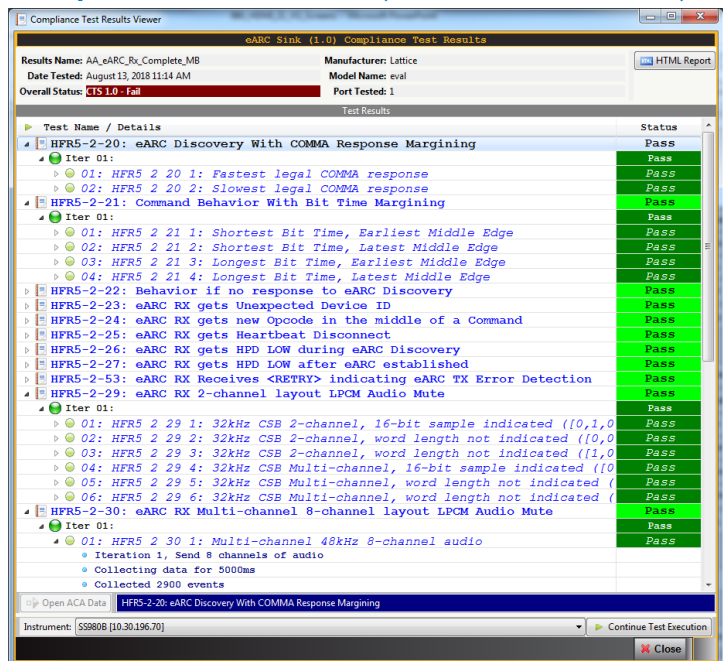
## eARC Compliance Testing

The M41h enables developers of HDMI eARC Tx and Rx devices to run compliance tests on their eARC-capable. The compliance tests run with little or no human interaction. Detailed results are provided for each test to help identify the root cause of failures. The reports can be exported and disseminated to colleagues and other subject matter experts.

## Test Suite (eARC Tx Test Suite Example Shown)



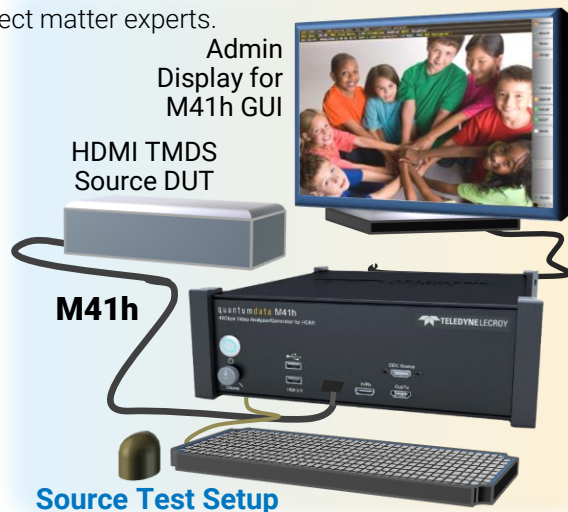
## Sample eARC Test Results (eARC Rx Tests Shown)



# HDMI 2.0 SOURCE, SINK TMDS COMPLIANCE TESTS

## HDMI TMDS Source Compliance

The M41h for HDMI Testing enables developers of HDMI source devices and silicon makers to run compliance tests on their TMDS source devices on streams at up to 4K video resolutions. All compliance test data, including the captured data, is exportable and can be disseminated to colleagues and other subject matter experts.



## HDMI TMDS Source – Partial List of Supported Tests

HDMI TMDS Source		
Instrument: MyM41h [10.30.196.32] Connect Cards		
CDF Entry Test Selection Test Options / Preview		
Select All	Duration	Options
EXECUTE TESTS		
TMDS Protocol		
HF1-10: TMDS Protocol - 6G - TMDS Bit Clock Ratio		✓
HF1-11: Source TMDS Protocol - 6G Legal Codes		✓
HF1-12: TMDS Protocol - 6G - Basic Protocol and Scrambling		✓
HF1-13: TMDS Protocol - Scrambling <= 3.4Gbps		✓
HF1-21: TMDS Protocol - 6G - Legal Codes - other Video Timings		✓
HF1-22: TMDS Protocol - 6G - Basic Protocol and Scrambling - Other Video Timings		✓
Pixel Encoding		
HF1-31: Pixel Encoding - YCBCR 4:2:0 - TMDS Pixel Encoding		✓
HF1-32: Pixel Encoding - YCBCR 4:2:0 Deep Color - TMDS Pixel Encoding		✓
Video Timing		
HF1-14: Video Timing - 6G - 2160p 24-bit Color Depth		✗
HF1-15: Video Timing - 6G - Deep Color		✓
HF1-16: Video Timing - 6G - 2160p 3D		✓
HF1-24: Video Timing - 6G - Other 24-bit Color Depth		✓
HF1-25: Video Timing - 6G - Other Deep Color		✓
HF1-26: Video Timing - 6G - Non-2160p 3D		✓
HF1-33: Video Timing - YCBCR 4:2:0		✓
HF1-34: Video Timing - YCBCR 4:2:0 Deep Color		✓
HF1-35: Video Timing - 21:9 (64:27)		✓

## HDMI TMDS Test Results – Video Tests

Compliance Test Results Viewer		
HDMI 2.1 Src (2.0) Compliance Test Results		
Results Name: HF1-25_VideoTiming_6G_HF1-18_AVI_IF_6G	Manufacturer: Teledyne LeCroy	HTML Report
Date Tested: January 11, 2017 9:43 AM	Model Name: Quantum Data 780E	
Overall Status: CTS 2.0 - Pass	Port Tested: 1	
Test Results		
Test Name / Details	Status	
HF1-25: Video Timing - 6G - Other Deep Color	Pass	
Iter 01: (63) 1920x1080p @ 120 Hz, DC - 36 bpp	Pass	
Iter 02: (64) 1920x1080p @ 100 Hz, DC - 36 bpp	Pass	
Iter 03: (77) 1920x1080p @ 100 Hz, DC - 36 bpp	Pass	
Iter 04: (78) 1920x1080p @ 120 Hz, DC - 36 bpp	Pass	
Iter 05: (91) 2560x1080p @ 100 Hz, DC - 36 bpp	Pass	
Iter 06: Any non-2160p DC Format, Max TMDS check	Pass	
HF1-18: AVI InfoFrame - 6G	Pass	
Iter 01: (96) 3840x2160p @ 50 Hz	Pass	
Iter 02: (97) 3840x2160p @ 60 Hz	Pass	
Iter 03: (101) 4096x2160p @ 50 Hz	Pass	
Iter 04: (102) 4096x2160p @ 60 Hz	Pass	
Iter 05: (106) 3840x2160p @ 50 Hz	Pass	
01: Verify AVI InfoFrame occurs at least once per two Video Fields	Pass	
02: Verify AVI InfoFrame version is equal to 2	Pass	
03: Verify AVI VIC is 0 for HDMI VICs	Pass	
04: Verify AVI VIC is correct for non-HDMI VICs	Pass	
05: Verify AVI PB1 bit 7 is 0	Pass	
06: Verify AVI PB4 bit 7 is 0	Pass	
07: Verify AVI PB14-PB27 bytes are 0	Pass	
Iter 06: (107) 3840x2160p @ 60 Hz	Pass	
Iter 07: (93) 3840x2160p @ 24 Hz, DC - 36 bpp	Pass	
Iter 08: (94) 3840x2160p @ 25 Hz, DC - 36 bpp	Pass	
Iter 09: (95) 3840x2160p @ 30 Hz, DC - 36 bpp	Pass	

## HDMI TMDS Sink Compliance

The M41h for HDMI Testing enables developers of HDMI sink devices and silicon makers to run compliance tests on their TMDS sink devices at up to 4K video resolutions. All compliance test data is exportable and can be disseminated to colleagues and other subject matter experts.



## HDMI TMDS Sink – Partial List of Supported Tests

HDMI TMDS Sink		
Instrument: MyM41h [10.30.196.32] Connect Cards		
CDF Entry Test Selection Test Options / Preview		
Select All	Duration	Options
EXECUTE TESTS		
TMDS Protocol		
HF2-5: TMDS Protocol - 6G - Scrambling		✓
HF2-9: TMDS Protocol - Scrambling <= 340Msc		✓
Pixel Decoding		
HF2-23: Pixel Decoding - YCBCR 4:2:0		✓
HF2-24: Pixel Decoding - YCBCR 4:2:0 Deep Color		✓
HF2-71: Pixel Decoding - YCBCR 4:2:0 for 861G Video Formats		✓
HF2-72: Pixel Decoding - YCBCR 4:2:0 Deep Color for 861G Video Formats		✓
EDID		
HF2-10: Video Timing - 6G - HF-VSDB		✓
HF2-26: EDID - Video Format Declaration		✓
HF2-31: EDID - YCBCR 4:2:0 - Data Blocks		✓
HF2-32: EDID - YCBCR 4:2:0 BT.2020 - Data Block		✓
HF2-35: EDID YCBCR 4:2:0 Deep Color HF-VSDB		✓
HF2-39: EDID 3D and Multi-stream Audio Data Blocks		✓
HF2-41: HDMI VSDBs - Independent-View		✓
HF2-53: EDID - HF-VSDB		✓
HF2-53: Sink Video Timing - FRL/Gaming/DSC - HF-VSDB		✓
HF2-70: Sink EDID - HF-VSDB Reserved Bits		✓
Timing 6G		
HF2-6: Video Timing - 6G - 2160p 24-bit Color Depth		✓
HF2-7: Video Timing - 6G - Deep Color		✓

## HDMI TMDS Test Results – Video Tests

Compliance Test Results Viewer		
HDMI 2.0 Sink (2.0) Compliance Test Results		
Results Name: Test_ID_2-7-1	Manufacturer: ACME	HTML Report
Date Tested: May 22, 2014 10:56 AM	Model Name: XYZ	
Overall Status: CTS 2.0 - Pass	Port Tested: 1	
Test Results		
Test Name / Details	Status	
HF2-7: Video Timing - 6G - Deep Color	Pass	
Iter 07: (93) 3840x2160p @ 24 Hz 16:9, 30 bpp	Pass	
Iter 08: (93) 3840x2160p @ 24 Hz 16:9, 36 bpp	Pass	
Iter 09: (93) 3840x2160p @ 24 Hz 16:9, 48 bpp	Skipped	
Iter 10: (94) 3840x2160p @ 25 Hz 16:9, 30 bpp	Pass	
Iter 11: (94) 3840x2160p @ 25 Hz 16:9, 36 bpp	Pass	
Iter 12: (94) 3840x2160p @ 25 Hz 16:9, 48 bpp	Skipped	
Iter 13: (95) 3840x2160p @ 30 Hz 16:9, 30 bpp	Pass	
Iter 14: (95) 3840x2160p @ 30 Hz 16:9, 36 bpp	Pass	
Iter 15: (95) 3840x2160p @ 30 Hz 16:9, 48 bpp	Skipped	

# HDCP 2.2 SOURCE, SINK, REPEATER COMPLIANCE TESTS

## HDCP 2.2 Compliance

The M41h HDCP 2.2 compliance tests are ideal for pre-testing your HDMI source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures.



## HDCP 2.2 Test Selection – Source Tests

HDMI HDCP 2.3 TX CT 1.0		
Instrument: MyM41h [192.168.1.21] Connect Cards		
CDF Entry	Test Selection	Test Options / Preview
Select All	✓ ✕	EXECUTE TESTS
TX with Receiver		
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	✓	
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	✓	
1A-03: Regular Procedure: Receiver disconnect after AKE_Init	✓	
1A-04: Regular Procedure: Receiver disconnect after Km	✓	
1A-05: Regular Procedure: Receiver disconnect after locality check	✓	
1A-06: Regular Procedure: Receiver disconnect after Ks	✓	
1A-07: Regular Procedure: Receiver sends REAUTH_REQ after Ks	✓	
1A-08: Irregular Procedure: Rx certificate not received.	✓	
1A-09: Irregular Procedure: Verify Receiver Certificate	✓	
1A-10: Irregular Procedure: SRM	✓	
Iter 01: This test has been deprecated: Automatic Not Judged	✓	
1A-11: Irregular Procedure: Invalid H'	✓	
Iter 01: Invalid H'	✓	
Iter 02: H' Timeout with previously paired Recv Id	✓	
Iter 03: H' Timeout with previously unpaired Recv Id	✓	
1A-12: Irregular Procedure: Pairing Failure	✓	
1A-13: Irregular Procedure: Locality Failure	✓	
Iter 01: Locality Failure	✓	
Iter 02: Locality Timeout	✓	
TX with Repeater		
1B-01: Regular Procedure: With Repeater	✓	

## HDCP 2.2 Test Results– Source Tests

HDMI HDCP 2.2 TX Compliance Test (1.0): "HDCP_22_Test"		
Test List		
Category / Test Name	Status	Status
Iter 01:	✓	Fail
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	✓	Fail
Iter 01:	✓	Fail
1A-03: Regular Procedure: Receiver disconnect after AKE_Init	✓	Pass
Iter 01:	✓	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	✓	Pass
Iter 01:	✓	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	✓	Pass
Iter 01:	✓	Pass
1A-07: Regular Procedure: Receiver sends REAUTH_REQ after Ks	✓	Pass
Iter 01:	✓	Pass
1A-11: Irregular Procedure: Invalid H'	✓	Pass
Iter 01: Invalid H'	✓	Pass
Iter 02: H' Timeout with previously paired Recv Id	✓	Pass
Iter 03: H' Timeout with previously unpaired Recv Id	✓	Pass
1A-12: Irregular Procedure: Pairing Failure	✓	Fail
Iter 01: Locality Failure	✓	Fail
Iter 02: Locality Timeout	✓	Pass

Line	Message
0001	Executing the test.
0002	Processing test results.
0003	Test 1A-13 Iter 01 -> Pass
0004	--- Test 1A-13-02
0005	Executing the test.
0006	Processing test results.
0007	Test 1A-13 Iter 02 -> Pass
0008	Tests completed

## HDCP 2.2 Test Selection – Sink Tests

HDMI HDCP 2.3 Receiver CT 1.0		
Instrument: ALM41d [10.30.196.30] Connect Cards		
CDF Entry	Test Selection	Test Options / Preview
Select All	✓ ✕	EXECUTE TESTS
Upstream with Transmitter		
2C-01: Regular Procedure - With transmitter	✓	
Iter 01: With previously not connected receiver	✓	
Iter 02: With previously connected receiver	✓	
2C-02: Irregular Procedure - New Authentication after AKE_Init	✓	
2C-03: Irregular Procedure - New Authentication during Locality Check	✓	
2C-04: Irregular Procedure - New Authentication after SKE_Send_Eks	✓	
2C-05: Irregular Procedure - New Authentication during Link Synchronization	✓	

## HDCP 2.2 Test Results – Sink Tests

Compliance Test Results Viewer		
HDMI HDCP 2.2 Receiver (1.0) Compliance Test Results		
Results Name: HDCP_22_Sink_Comp_1		Manufacturer: Acme
Date Tested: October 3, 2014 9:50 AM		Model Name: XYZ
Overall Status: <b>CTS 1.0 - Fail</b>		Port Tested: 1
Test Results		
Test Name / Details	Status	Status
2C-01: Regular Procedure - With transmitter	✓	Pass
2C-02: Irregular Procedure - New Authentication after AKE_Init	✓	Pass
2C-03: Irregular Procedure - New Authentication during Locality Check	✓	Pass
Iter 01:	✓	Pass
ERROR: ioctl QDIOVC_TX_DDC_READ failed. Error: '-1'	✗	Fail
ERROR: I2C 74:70 READ error: '-1'	✗	Fail
MSG:HFD_DIS ts:0x115f36 us	✓	Pass
MSG:VALID_VER ts:0x0 us	✓	Pass
MSG:HFD_EN ts:0x330 us	✓	Pass
TX:UNAUTH:enter	✓	Pass
AKE_INIT ts:0xf5339 us	✓	Pass
MSG RCVD:AKE_Send Cert ts:0xf5613 us	✓	Pass
Snd No Stored_KM ts:0x13fa9 us	✓	Pass
MSG RCVD:AKE_Send_H_Prime ts:0x171f29 us	✓	Pass
MSG RCVD:AKE_Send_pairing_info ts:0x1742fb us	✓	Pass
Snd LC_Init ts:0x175e0d us	✓	Pass
MSG RCVD:LC_Send_L_Prime ts:0x1767b7 us	✓	Pass
Snd SKE_Send_EKS ts:0x179943 us	✓	Pass
TX:AUTH:enter	✓	Pass
2C-04: Irregular Procedure - New Authentication after SKE_Send_Eks	✓	Pass
2C-05: Irregular Procedure - New Authentication during Link Synchronization	✓	Fail
Iter 01:	✓	Fail
ERROR: ioctl QDIOVC_TX_DDC_READ failed. Error: '-1'	✗	Fail
ERROR: I2C 74:70 READ error: '-1'	✗	Fail
MSG:HFD_DIS ts:0xc7b4b8 us	✓	Pass
MSG:VALID_VER ts:0x0 us	✓	Pass
MSG:HFD_EN ts:0x32a us	✓	Pass
TX:UNAUTH:enter	✓	Pass
AKE_INIT ts:0xeb8d2f9c us	✓	Pass
2C-01: Regular Procedure - With transmitter		
Instrument: [55.980 [192.168.254.153]		
Continue Test Execution		



# SPECIFICATIONS **UPDATES!**

## HDMI Capabilities

Version	Up to HDMI 2.1
Standard Formats	CEA, VESA
Protocols	FRL with FEC, DSC; TMDS, HDCP 1.4, HDCP 2.3, eARC
FRL bit rates	3Gbps; 6Gbps; 8Gbps; 10Gbps; 12Gbps (48Gbps aggregate)
Max Pixel Rate	2376MHz
Capture memory	8 GBytes

## Connectors - Front

HDMI Connectors (2)	In/Rx HDMI Type A; Category 2 Out/Tx HDMI Type A: Category 2
DDC Source	Used for eARC Tx EDID test
USB (2)	For connecting keyboard/mouse for ATP Manager control or external storage

## Connectors - Back

HDMI - Admin Connector	HDMI Port for M41h ATP Manager for external 4K UHD TV at Admin HDMI port
USB (2); USB-C (2)	Keyboard / mouse connected to USB ports;
RJ45 E1	For admin control over LAN from computer running M41h ATP Manager
RCA (2)	SPDIF IN for injecting audio; SPDIF OUT for extracting incoming audio
BNC (2)	Trigger IN / OUT for triggering captures
All other connectors	Not used

## Physical / Electrical / Admin

Power	100-240 VAC, 50-60 Hz, 200 Watts
Weight	11.15 LBS; 5.057 Kg
Size	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm)
Rack mountable	2 RU mounts in 19 inch rack with rack mounting brackets (provided)
Internal speaker	Speaker with volume control for monitoring incoming audio
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
GUI Control	Either through External PC connected over LAN to Ethernet RJ45 or: Keyboard / mouse connected to USB ports; External 4K UHD TV at Admin HDMI port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

## Ordering - Product Code

## Description

00-00258	M41h hardware and base functional tester – Includes Video Generation, Basic Analysis and Aux Channel Analyzer (ACA)
95-00209	M41x rack-mount kit
95-00195	Source Enhanced Functional test – Includes Capture Analysis, Gaming Compliance, DSC Functional testing, HDR10+ and Cable ID Compliance and UHDA Compliance Tests
95-00201	Sink Enhanced Functional test – Includes UHDA Patterns, DSC Functional Test, CEC ITE & Gaming and Cable ID Compliance Tests
95-00230	Passive DDC monitoring in FRL mode (requires custom cable)
95-00204	eARC Tx (Sink) functional test
95-00199	eARC Rx (Source) functional test
95-00196 <b>UPDATES</b>	FRL & DSC Source compliance tests (req's 95-00195) <b>Tests added &amp; enhanced</b>
95-00202 <b>UPDATES</b>	FRL & DSC Sink compliance tests (req's 95-00201) <b>Tests added &amp; enhanced</b>
95-00205	eARC Tx (Sink) compliance tests (required 95-00204)
95-00200	eARC Rx (Source) compliance tests (requires 95-00199)
95-00198	HDCP 2.2 Source compliance (requires 95-00195)
95-00206	HDCP 2.2 Sink compliance (requires 95-00201)
95-00197	TMDS Source compliance tests (requires 95-00195)
95-00203	TMDS Sink compliance tests (requires 95-00201)
95-00207 <b>UPDATES</b>	Sink HDR Tests (Dolby, HDR Lab [ <b>Updated to 8K</b> ]) (requires 00-00258)





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