

Envision X84 CSI & DSI Protocol Analyzer & Exerciser for MIPI CSI-2v2 and DSI-2 with Analyzer Conformance Testing



Envision X84 Exerciser

With comprehensive support for MIPI CSI-2 and DSI-2 specifications, Teledyne LeCroy's Envision X84 combination Analyzer and Exerciser platform provides the industry's most complete, accurate and reliable test solution for MIPI silicon makers and integrators.

Envision X84 Analyzer

The Envision X84 Analyzer capture utility provides deep analysis for both MIPI camera and display protocols. The X84 Analyzer can be positioned either as an endpoint to test a CSI/DSI stream or tapped in between a CSI/DSI device and host for passive monitoring and analysis. The X84 ensures fast Time-to-Insight through its rich set of innovative features for debug analysis and identifying and resolving elusive protocol errors.

The Envision X84 Analyzer offers an optional integrated MIPI Conformance Test Specification (CTS) suite for both CSI and DSI. This CTS suite provides checks across all camera and display modes, packet types, and video formats, including high speed and low-power modes.

Key Features & Benefits - X84 Analyzer

- Compliant with MIPI Display Serial Interface (DSI v2.0) Specification – Capture all packet types and data formats, command and video modes, high speed and low power read and write modes, and DCS supported.
- Display Stream Compression (DSC) Optional feature to decode incoming DSC encrypted content from a DSI host including parsing the PPS metadata parameters.
- Compliant with MIPI Camera Serial Interface (CSI-2v2) Specifications – Analyze all packet types and data formats, including video frames and timing.
- 2.5 Gbps D-PHY data transfer rate per data lane Scalable from 1-4 data lanes.
- 2.5 GSps C-PHY data transfer rate per data lane Scalable from 1-3 data lanes (2.28 bits per sample).
- passively tapped between device and host or capturing traffic as a DSI or CSI sink.
- Detailed protocol checking PHY-level and protocol level events including low-power, high speed bursts and read/writes.
- Complex event-based transaction capture with 2.5ns event timing resolution for detailed self-checking and debug.
- Statistics for received data and errors For off-line debug and analysis.
- External Trigger In / Out Trigger external equipment based on packet structures or event.
- Conformance Test Suite Optional CTS for CSI-2v2 and DSI-2, for evaluating your device against specifications.

MIPI Display Serial Interface (DSI v2.0) Specification -Generate a sequence of images and frames at

Interface (CCI) responses.

timinas.

various resolutions and timings. D-PHY support at 2.5 Gbps data transfer rate per data lane - Scalable from 1-4 lanes.

Teledyne LeCroy's Envision X84 Exerciser (video

generator) is a versatile and flexible tool for MIPI

camera and display protocols. Like the X84 Analyzer,

the Exerciser is offers rich suite of innovative features

for generating DSI and CSI packets, frames and

images. The Exerciser can be configured to generate

sequences of packets or multiple images at various resolutions, color modes, sampling rates and frame

Key Features & Benefits – X84 Exerciser

MIPI Camera Serial Interface (CSI-2) Specifications -

Create and generate all packet types, data formats

and frame timing. Also generate Camera Control

- C-PHY supports 2.28 Symbols per second per trio -Scalable from 1-3 trios or data lanes.
- **Detailed protocol checking PHY-level and protocol** level events including low-power and writes/reads.
- Event Based generation with 2.5ns event resolution.
- Advanced Triggering Start and stop generate on protocol events, data patterns, and external triggers.
- External Trigger In / Out Use the Teledyne LeCroy X84 to generate any event and toggle a scope or logic analyzer (via SMA connectors).
- Automation API for advanced test creation.

Automation API for advanced test creation.

This highly configurable, single platform solution is ideal for MIPI camera and display testing. The Envision X84 is the intelligent choice for any camera and display validation needs.

ENVISION X84 - ANALYZER

Flexible Hardware Platform

The front-end of the Envision X84 analyzer features standard MMCX connectors that support C-PHY or D-PHY signals to provide high fidelity capture of traffic from all active lanes simultaneously. Concurrent recording of PHY-level and protocol-level events allows viewing of per-lane and protocol activity to help characterize and debug interface traffic. The Envision X84 Analyzer platform includes 6GB of recording memory plus a GbE link for uploading recorded traffic to the host PC.

The heart of the Envision X84 Analyzer is a patented Test IP Transaction Processor technology. This state-of-the-art protocolprocessing core incorporates a real-time recording engine and configurable tools to selectively monitor and record MIPI CSI and DSI traffic. Field upgradeable firmware allows the Transaction Processor to evolve and support new features or future changes to the MIPI CSI and DSI specifications.

The built-in triggering provides unprecedented flexibility with every possible packet type and error counts, including combinations, configurable as a trigger event. In wrap recording mode, the Envision X84 captures continuously and provides debug back tracing of events for extended debug sessions. All triggers can also generate an external trigger event for synchronizing external scopes or other instruments. An input trigger is useful for coordinating analysis with external events.

A General Purpose I/O (GPIO) connector is included for connection to the CSI or DSI device under test. This can be used for control and status. For CSI, two pins are used as Camera Control Interface (CCI). All pins are controllable via the software GUI or instrument API.

Analysis Software

The Envision X84 utilizes a software application to control the instrument. A user API is also available for automated testing if desired. The user interface uses colors and patterns to train the eye to understand information faster. When recording mixed protocol and PHY traffic, packets are color coded and interleaved in a single display.

CSI Test Configuration – Host Emulation Mode

In CSI host emulation mode, the X84 Analyzer acts as a MIPI Host connected to a camera or image sensor device under test (DUT) that provides the MIPI device interface.



CSI Test Configuration – Passive Probing Mode

In the CSI passive probing mode, the X84 Analyzer is positioned as a passive tap between a CSI host SoC and a CSI camera to sniff traffic. This application is invaluable where the transmission path undergoes a format conversion or traverses a transport facility. By positioning the X84 passive probe elements at various points along the transport facility, the X84 can segment and isolate the point of failure.

DSI Test Configuration – Device Emulation Mode

In DSI device emulation mode, the X84 Analyzer acts as a MIPI Display device connected to an SoC device under test (DUT) that provides the MIPI Host interface.



DSI Test Configuration – Passive Probing Mode

In the DSI passive probing mode, the X84 Analyzer is positioned as a passive tap between a DSI host SoC and a DSI display device to sniff traffic. This application is invaluable where the transmission path undergoes a format conversion or traverses a transport facility. By positioning the X84 passive probe elements at various points along the transport facility, the X84 can segment and isolate the point of failure.



ENVISION X84 - ANALYZER

Envision X84 CSI/DSI Analyzer Protocol Test Suite

The Teledyne LeCroy Envision CSI/DSI Protocol Test Suite's Events tab shows each packet or PPI event on a separate row with every field labeled and color-coded. Events can be individually filtered, searched or exported from the captured trace.

For each capture, Event Statistics are shown in the summary area (top right on screen examples). The examples show cases with both Phy and protocol elements (right) and only protocol packets (below) in this case both Long and Short protocol packets. The Capture configuration that is used to acquire a capture is also provided (Capture Setup upper middle [right]).

The Event Filters area enables users to include/exclude types of protocol traffic from the various analysis tabs (Events, Video, Video Analysis, Timing, Errors). Predefined filters are available as well as a user-defined filter mechanism, to facilitate quick Time-to-Insight into problem areas.

Quick setup buttons enable start or stop captures, select the number of lanes, and set or detect PHY speed.

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| 10 | 542.500 nS | 2.500 pS | | | | | State Lane 2 | | | | | |
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| 18 | 1.027 uS | 2.500 nS | | | | | Mode Lane 0 | | | | | |
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Update Time: 0.1 secs

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Intelligent Triggering

Teledyne LeCroy Envision CSI Protocol Suite - Event File: Ferrari

The Envision X84 Analyzer provides hardware triggering to ensure particular protocol events of interest are captured. Trigger events can be specified at the protocol level, targeting specific protocol structures, counts and errors. External triggers from a scope for example can also be used to initiate a capture.



ENVISION X84 – VIDEO & TIMING ANALYSIS

Video Analysis

The Envision X84 Analyzer can capture and analyze all standard video and image types outlined in the MIPI CSI-2 and DSI-2 specifications. Images can be extracted and displayed for viewing on the Video tab as shown (right). The captured images can also be compared to "golden images" or validated in "Loop" mode with a Stop on Errors. The Video tab shows the color type (e.g. RGB, YUV), the chroma sampling mode (e.g. 4:4:4, 4:2:2), the frame rate and the resolution of the incoming video stream that was captured.





Video Frame Analysis

The Envision X84 Analyzer provides a summary view of the timing parameters and frame structure including the line and frame blanking and the front and back porch (left). The Video Analysis feature depicts the frame structure showing the active video and the blanking. The frame blanking is expressed in lines and line blanking expressed in bytes. A summary window lists the primary video frame parameters and their values.

Timing Diagram

The Envision X84 Analyzer depicts timing elements as the CSI or DSI stream transitions from Low Power mode to the High Speed burst mode (right). The Timing Diagram tab shows the timing for each transition. The relevant timing parameters are averaged over the frames capture and are presented along with the minimum and maximum times.

Timing Analysis (see next page)



ENVISION X84 – ANALYZER CONFORMANCE TESTING

Conformance Testing

The Envision X84 Analyzer offers a Conformance Test Suite (CTS) of the various protocol levels and elements of an incoming video stream. The CTS provides a quick assessment to help ensure that your device meets the requirements. The conformance suite provides pass/fail indication including partial results.





One-button Operation

The Conformance Test Suite (CTS) feature offers a one touch initiation. The CTS test suite analyzers one or more event files to determine conformance.

The application allows point-and-click selection of individual test cases to view results. Users can export test results to a spreadsheet or a CSV file.

The examples shown on this page provide a list of the individual tests in the CTS test suite. The test coverage is broad including data and clock, and protocol bytes including short and long packet structure, frame structure, timing, etc.



Timing Analysis

The Envision X84 Analyzer enables users to verify time comparisons between user specified CSI or DSI protocol elements. For example, you can view the minimum, maximum and average elapsed time between frame start and end, line start and line end, payload burst and blanking, etc.

ENVISION X84 – EXERCISER

Flexible Hardware

The Envision X84 platform conforms to the MIPI DSI and DSI-2 and the CSI-2 version 2 standards and supports both C-PHY & D-PHY standards.

The front-end of the Envision X84 Exerciser features standard MMCX connectors that support C-PHY or D-PHY signals to provide high fidelity generation of traffic from all active lanes simultaneously. Concurrent recording of PHY-level and protocol-level events during generation allows viewing of per-lane and protocol activity to help characterize and debug interface traffic going to the DUT. The Envision X84 platform includes 4GB of memory for images.

The heart of the Envision X84 Exerciser is a patented Test IP Transaction Processor technology. This state-of-the-art protocolprocessing core incorporates a real-time generation and recording engine and configurable tools to selectively monitor and generate MIPI CSI and DSI traffic. Field upgradeable firmware allows the Transaction Processor to evolve and support new features or future changes to the MIPI CSI and DSI specifications.

The built-in triggering provides unprecedented flexibility to start and stop generation with every possible packet type configurable as trigger events. In Loop mode, the Envision X84 generates packets and video continuously for extended debug sessions

As the Envision X84 Exerciser generates traffic, it can be configured to also generate an external trigger on any packet or frame type. This trigger event can be used for synchronizing external scopes or other instruments. An input trigger is useful for starting and/or stopping generation.

Envision X84 Software

The Envision X84 utilizes a software graphical interface to control the instrument. A user API is available for automated testing if desired. For each generation case, event statistics are shown on the summary area on the top right. Selected triggers are shown on the middle right, to quickly view the setup selected. Quick setup buttons are at the top left to start or stop generation, select the number of lanes, and set or detect PHY speed.

CSI Test Configuration – Camera Emulation Mode

In CSI Camera emulation mode, the X84 Exerciser acts as a MIPI CSI image Sensor/Camera connected to a CSI Host/Image Processor under test (DUT).



Envision X84 CSI Camera (Image Sensor)

(CSI Host SoC)

DSI Test Configuration – Host Emulation Mode

In DSI Host emulation mode, the X84 Exerciser acts as a MIPI DSI Host SoC connected to a DSI Display Device under test (DUT).



ENVISION X84 – EXERCISER

Generation Modes

The Envision X84 Exerciser can generate all standard video and image types outlined in the MIPI CSI-2 and DSI-2 specifications. This enables you to emulate a variety of image sensors and parameters over multiple lane configurations. The Exerciser handles the lane deskewing necessary where multiple lanes are used.

The Envision X84 Exerciser software application allows the user to generate traffic in two different modes: Video Mode or Packet Mode. By using the simple drag and drop methodology, users can quickly generate their desired traffic.

Video Generation Mode

In the Video mode, users can pick and choose different frame types and define a specific image, either in binary format (.bin) or in bitmap (.bmp) format. The Envision X84 Exerciser will then create all the packets necessary to deliver a valid frame.

The user can define frame timing and resolution for each sequence of images. H-Sync and V-Sync timing can also be defined for generation.

Packet sequences and video frames can be sent as a single transmission or can be looped to generate continuous traffic. Frames can also be sequenced and/or repeated.

Packet Generation Mode

In Packet Mode, the user can select from standard packet types and define a single packet or a sequence of packets. Each packet can be modified for content as well as frame timing and resolution. Metadata packets can be sent in the blanking. Error conditions can be created with short packets for stress testing a device.

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| Packets Frame Packets Frame Packets Frame End Lune Stat Lune Stat Lune Stat Common State Packets Frame Packets Fra | S | Step Name Step Name Nep Step Name Nep Name Nep Name Nep Name Step Name | Packet Type Shot Pik 1 Barking Pik Frame Stat Line Stat RoB830 tak Frame End Barking Shot Pik 2 Shot Pik 1 0 (b.0000 | Data ID Data I 0x08 Defa 0x00 Defa 0x00 Defa 0x02 Defa 0x02 Defa 0x11 Defa 0x09 Defa 0x09 Defa | uit 0 uit 0 ui | Gx0000 0 0x0000 0 0 0x0000 0 0 | 0x0E 0x14 0x00 0x08 0x18 0x07 0x14 | 0x00 0x00 0x00 0x00 0x00 0x00 0x00 | 0x08 0x11 0x00 0x02 0x24 0x01 0x11 | 0x00 Word Count: 0 0x00 Word Count: 0 0x00 Word Count: 0 | 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 |
| Packets Frame Packets Frame Stat Frame Stat Frame End Lune Stat Lune Stat Lune Stat Stat Banking Pit Genered State Packets Stat Stat Stat Stat Stat Stat Stat St | S C | Step Name Step Name | Packet Type Short Pit 1 Barking Pit Frame Stat Frame End Barking Pit Short Pit 1 | Data ID Data I 0x08 Defa 0x00 Defa 0x00 Defa 0x02 Defa 0x02 Defa 0x11 Defa 0x09 Defa 0x09 Defa | uit 0 uit 0 ui | Gx0000 0 0x0000 0 0 0x0000 0 0 | 0x0E 0x14 0x00 0x08 0x18 0x07 0x14 | 0x00 0x00 0x00 0x00 0x00 0x00 0x00 | 0x08 0x11 0x00 0x02 0x24 0x01 0x11 | 0x00 Word Count: 0 0x00 Word Count: 0 0x00 Word Count: 0 | 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 |
| Packets Frame Packets Frame Packets Frame Stat Frame Frame Stat Frame Frame Stat Frame Fr | S | Step Name Step Name Nep Step Name Nep Name Nep Name Nep Name Step Name | Packet Type Shot Pik 1 Barking Pik Frame Stat Line Stat RoB830 tak Frame End Barking Shot Pik 2 Shot Pik 1 0 (b.0000 | Data ID Data I 0x08 Defa 0x00 Defa 0x00 Defa 0x02 Defa 0x02 Defa 0x11 Defa 0x09 Defa 0x09 Defa | uit 0 uit 0 ui | Gx0000 0 0x0000 0 0 0x0000 0 0 | 0x0E 0x14 0x00 0x08 0x18 0x07 0x14 | 0x00 0x00 0x00 0x00 0x00 0x00 0x00 | 0x08 0x11 0x00 0x02 0x24 0x01 0x11 | 0x00 Word Count: 0 0x00 Word Count: 0 0x00 Word Count: 0 | 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 |
| Packets Frame Packets Frame Start Frame Start Frame End Lune Start Lune Start Lune Start Lune Start Banking Pit Genner Stort Packets Start Pit Start S | S C | Step Name Step Name Nep Step Name Nep Name Nep Name Nep Name Step Name | Packet Type Shot Pik 1 Barking Pik Frame Stat Line Stat RoB830 tak Frame End Barking Shot Pik 2 Shot Pik 1 0 (b.0000 | Data ID Data I 0x08 Defa 0x00 Defa 0x00 Defa 0x02 Defa 0x02 Defa 0x11 Defa 0x09 Defa 0x09 Defa | uit 0 uit 0 ui | Gx0000 0 0x0000 0 0 0x0000 0 0 | 0x0E 0x14 0x00 0x08 0x18 0x07 0x14 | 0x00 0x00 0x00 0x00 0x00 0x00 0x00 | 0x08 0x11 0x00 0x02 0x24 0x01 0x11 | 0x00 Word Count: 0 0x00 Word Count: 0 0x00 Word Count: 0 | 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 |

| | ſ | Frame T | iming Configu | ration File | |
|------------|--------------------|--------------|---------------|-------------------|----------|
| Config | uration | RAW10_1920 | ×1080 | ✓ Save | Manage |
| | Frame Se | ettings | | | |
| | | Pixels | 10 | Lines | |
| | HSync | 500 | VSync | 45 | |
| | HActive | 1920 | VActive | 1080 | |
| Packets | | e LS/LE Pack | Tim | ing | _ |
| - | | | | Line Time (us) | 13.4556 |
| 1112041200 | Numbering | | ~ | Pixel Clk (MHz) | 180.0000 |
| Line | Numbering | Yes | ~ | Frame Rate (Hz) | 66.1199 |
| HSyn | c Blanking | Use LP11 | ~ H | S Sym Rate (Mbps) | 920 |
| Vertica | al Blanking | Use LP11 | ~ | Video Forma | et 🛛 |
| - CILING | ar under inder ing | USE LP II | 100 | RAW10 Data | 4 |

SPECIFICATIONS

General

| Protocols Supported | MIPI CSI-2v2, MIPI DSI-2 |
|-----------------------------|--|
| Data Rates – C-Phy | 3G Symbols per second; 1-3 trios of data lanes |
| Data Rates – D-Phy | 2.5Gbps; 1-4 lanes |
| Analyzer Recording Memory | 4-8GBytes |
| Exerciser memory for images | 4Gbytes |

Connectors – Front Panel

| D-PHY & C-PHY Interconnection | (12) MMCX Jack |
|-------------------------------|---|
| | D-Phy (4) Lanes: D0+/- D1+/- D2+/- D3+/- CK+/- |
| | C-Phy (3) Lanes: A0 B0 C0; A1 B1 C1; A2 B2 C2; |
| | Mates with MMCX Straight Male (plug) |
| GPIO Connector: | Molex I-Grid 2x10 connector, Part Number 5018762040 |
| | Mates with Molex I-Grid 2x10 Cable Connector, |
| | Part Number: 501646-2000 and up to (20) Crimp Contacts, |
| | Part Number: 501647-1000 |
| | Electrical Specifications: |
| | Bi-Directional GPIO |
| | Number of I/O Lines: 7 |
| | Voh: Open Collector Outputs, |
| | Require pull-up resistors to +1.8V - Vpu </5.0V.</td |
| | Vol: +0.6V Max.@ 8mA, |
| | Vih: +1.2V Min. +5.0V Max., Vil: +0.6V Max. |
| | +3.3V @ 1.5A Output Power |
| | I2C Communication Bus |
| | Open Drain with +3.3V 5K Pull-Up Resistors |
| | 400kHz |
| | SMA Jack Input |
| Trigger IN Connector: | Impedance: 700 Kohms |
| rigger in connector. | Max. Input Voltage: +3.5V |
| | Vih: +2.0V Min., Vil: +0.8V Max |
| | SMA Jack Output Impedance: 50 ohms |
| Trigger OUT Connector: | Max. Input Voltage: +3.3V |
| | Voh: +2.3V Min. @ 12mA |

Physical/Electric/Admin

| Dimensions (W x H x D) | 16.0" x 1.75" x 12.75" (40.64 cm x 4.45 cm x 23.9 cm) | |
|------------------------|--|--|
| Weight | 6.0 lbs (2.72kg) | |
| Environmental | Operating Temperature: 0°C to 50°C (32°F to 122°F) Non-Operating Temperature: -10°C to 80°C (14°F to 176°F) Operating Temperature: 0°C to 55°C (32°F to 131°F) Humidity: 10% to 90% RH (non-condensing) | |
| Power Requirements | External 120-220V AC Power | |
| Warranty | 12 Months Hardware Warranty | |

Ordering/Product Code Des

| D | 1.4.4 |
|----------|-------|
| Descri | ntion |
| Descri | |

| ENV-CD01-TAA-X | Envision X84 Hardware |
|-----------------|----------------------------------|
| ENV-CD01-ANA-A | Envision X84 Analyzer License |
| ENV-CD01-GEN-A | Envision X84 Generator License |
| ENV-CD01-CPHY-A | Envision X84 - C-PHY License |
| ENV-CD01-DPHY-A | Envision X84 - D-PHY License |
| ENV-CD01-CSI-A | Envision X84 - CSI License |
| ENV-CD01-DSI-A | Envision X84 - DSI License |
| ENV-CD01-GPIO-A | Envision X84 – GPIO/CCI License |
| ENV-CD01-DSC-A | Envision X84 - DSC License |
| ENV-CD01-CSC-A | Envision CSI Compression License |
| | |







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绿测科技有限公司

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